

SRM2B256SLMX55/70/10

256K-BIT STATIC RAM

- **Wide Temperature Range**
- **Extremely Low Standby Current**
- **Access Time 100ns (2.7V) 55ns (4.5V)**
- **32,768 Words × 8-Bit Asynchronous**

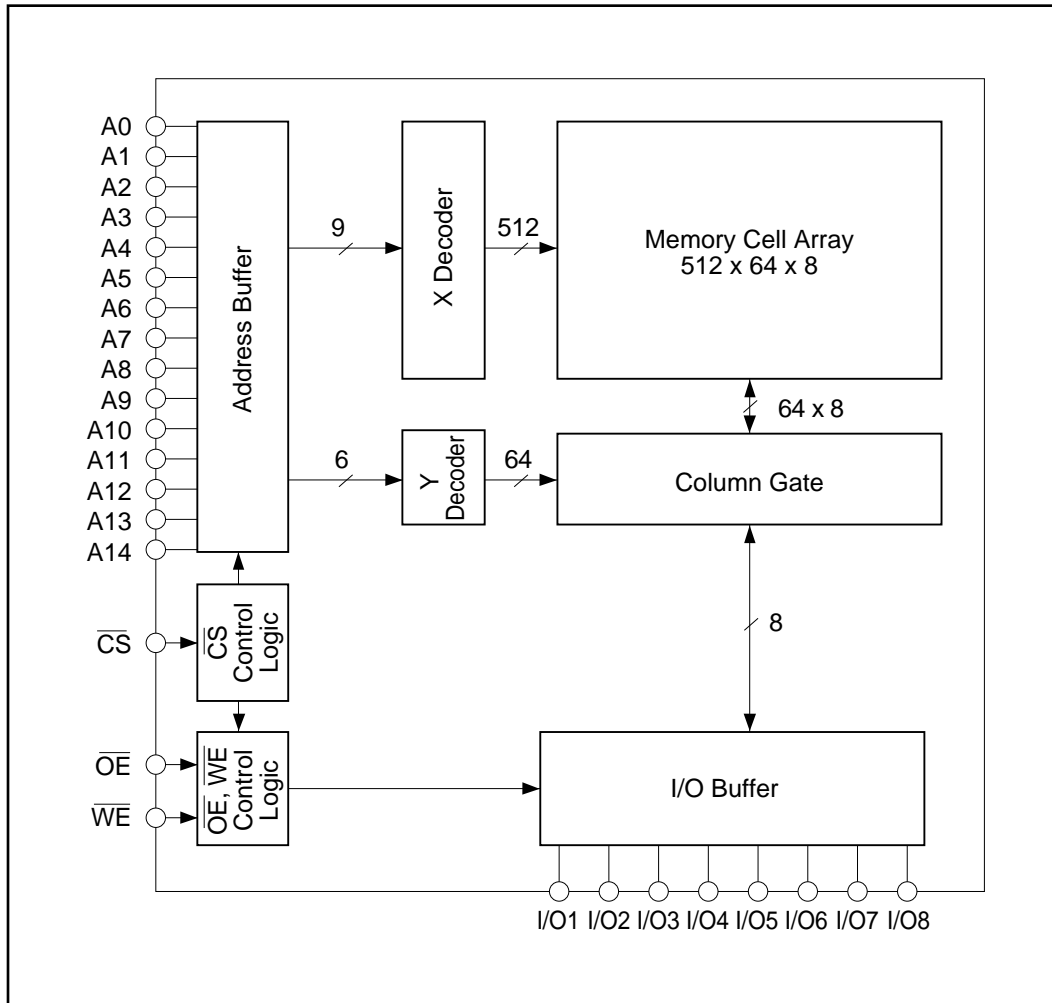
■ DESCRIPTION

The SRM2B256SLMX is a low voltage operating 32,768 words × 8-bit asynchronous, static, random access memory fabricated using an advanced CMOS technology. Its very low standby power consumption makes it ideal for applications requiring non-volatile storage with back-up batteries, and -25 to 85°C operating temperature range makes it ideal for industrial use. The asynchronous and static nature of the memory requires no external clock or refresh circuit. 3-state output ports allow easy expansion of memory capacity. These features make the SRM2B256SLMX usable for a wide range of applications, from microprocessor systems to terminal devices.

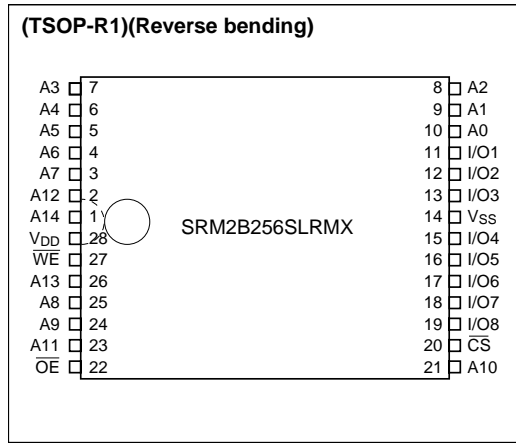
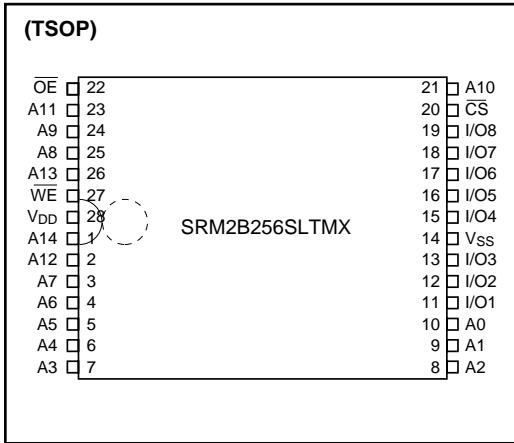
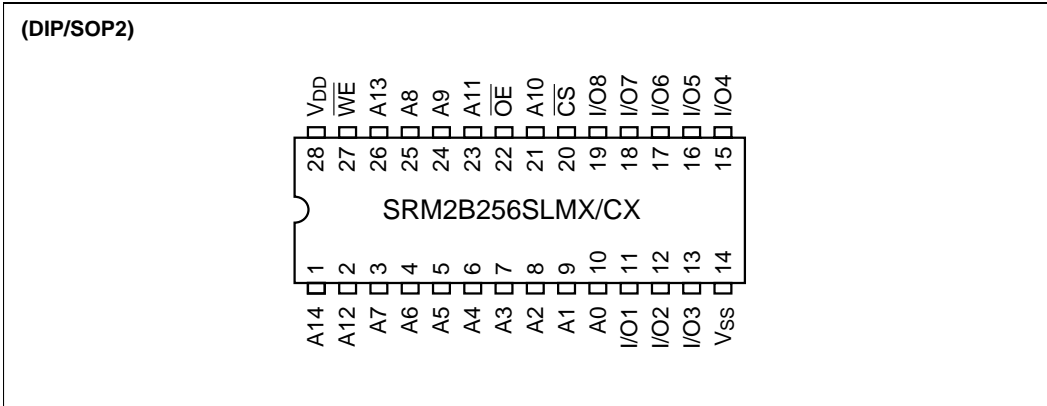
■ FEATURES

- Wide temperature range -25 to 85°C
- Extended supply voltage range. 2.7 to 5.5V
- Fast access time. 100ns (3V ± 10%)
55ns (5V ± 10%)
- Extremely low standby current SL Version
- Completely static. No clock required
- 3-state output
- Battery back-up operation
- Package SRM2B256SLCX DIP2-28pin (plastic)
SRM2B256SLMX SOP2-28pin (plastic)
SRM2B256SLTMX TSOP (I)-28pin (plastic)
SRM2B256SLRMX TSOP (I)-28pin-R1 (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A14	Address input
\overline{WE}	Write Enable
\overline{OE}	Output Enable
\overline{CS}	Chip Select
I/O1 to I/O8	Data I/O
VDD	Power Supply (2.7V to 5.5V)
VSS	Power Supply (0V)

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■ ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage	V _{DD}	-0.5 to 7.0	V
Input voltage	V _I	-0.5* to 7.0	V
Input/output voltage	V _{I/O}	-0.5* to V _{DD} + 0.3	V
Power dissipation	P _D	1.0	W
Operating temperature	T _{OPR}	-25 to 85	°C
Storage temperature	T _{STG}	-65 to 150	°C
Soldering temperature and time	T _{SOL}	260°C, 10s (Lead only)	—

* V_I, V_{I/O} (Min.) = -3.0V when pulse width is less or equal to 50ns

■ DC RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0V, T_a = -25 to 85°C

Parameter	Symbol	V _{DD} = 3V ± 10%			V _{DD} = 5V ± 10%			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V _{DD}	2.7	—	3.3	4.5	—	5.5	V
	V _{SS}	0	—	0	0	—	0	V
Input voltage	V _{IH}	2.2	—	V _{DD} + 0.3	2.2	—	V _{DD} + 0.3	V
	V _{IL}	-0.3*	—	0.4	-0.3*	—	0.8	V

* V_{IL} (Min.) = -3V when pulse width is less or equal to 50ns

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{SS} = 0V, T_a = -25 to 85°C)

Parameter	Symbol	Conditions	V _{DD} = 3V±10%			V _{DD} = 5V±10%			Unit
			Min	Typ*1	Max	Min	Typ*2	Max	
Input leakage	I _{LI}	V _I = 0 to V _{DD}	-1	—	1	-1	—	1	μA
Standby supply current	I _{DDS}	$\overline{CS} = V_{IH}$	—	—	2	—	—	3.0	mA
	I _{DDS1}	$\overline{CS} \geq V_{DD} - 0.2V$	—	0.3	25	—	0.5	50	μA
Average operating current	I _{DDA}	V _I = V _{IL} , V _{IH} I _{I/O} = 0mA, t _{CYC} = Min	—	10	15	—	30	45	mA
	I _{DDA1}	V _I = V _{IL} , V _{IH} I _{I/O} = 0mA, t _{CYC} = 1μs	—	—	5	—	—	10	mA
Operating supply current	I _{DDO}	V _I = V _{IL} , V _{IH} I _{LO} = 0mA	—	—	5	—	—	10	mA
Output leakage	I _{LO}	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, V _{I/O} = 0 to V _{DD}	-1	—	1	-1	—	1	μA
High level output voltage	V _{OH}	I _{OH} = -1.0mA, -0.5mA*3	2.4	—	—	2.4	—	—	V
Low level output voltage	V _{OL}	I _{OL} = 2.1mA, 1.0mA*3	—	—	0.4	—	—	0.4	V

*1 Typical values are measured at T_a = 25°C and V_{DD} = 3.0V*2 Typical values are measured at T_a = 25°C and V_{DD} = 5.0V*3 V_{DD} = 3.0V±10%

● Terminal Capacitance

(f = 1MHz, T_a = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address capacitance	C _{ADD}	V _{ADD} = 0V	—	—	8	pF
Input capacitance	C _I	V _I = 0V	—	—	8	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	10	pF

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● AC Electrical Characteristics

○ Read Cycle

V_{SS} = 0V, T_a = -25 to 85°C

Parameter	Symbol	Condi- tions	SRM2B256SLMX55		SRM2B256SLMX70		SRM2B256SLMX10		Unit						
			V _{DD} = 3V ±10%		V _{DD} = 5V ±10%		V _{DD} = 3V ±10%			V _{DD} = 5V ±10%					
			Min.	Max.	Min.	Max.	Min.	Max.		Min.	Max.				
Read cycle time	t _{RC}	*1	100	—	55	—	120	—	70	—	180	—	100	—	nS
Address access time	t _{ACC}		—	100	—	55	—	120	—	70	—	180	—	100	nS
$\overline{\text{CS}}$ access time	t _{ACS}		—	100	—	55	—	120	—	70	—	180	—	100	nS
$\overline{\text{OE}}$ access time	t _{OE}		—	60	—	30	—	70	—	35	—	90	—	45	nS
$\overline{\text{CS}}$ output set time	t _{CLZ}	*2	15	—	10	—	15	—	10	—	15	—	10	—	nS
$\overline{\text{CS}}$ output floating	t _{CHZ}		—	35	—	20	—	40	—	25	—	50	—	35	nS
$\overline{\text{OE}}$ output set time	t _{OLZ}		5	—	0	—	5	—	0	—	5	—	0	—	nS
$\overline{\text{OE}}$ output floating	t _{OHZ}		—	35	—	20	—	40	—	25	—	50	—	35	nS
Output hold time	t _{OH}	*1	15	—	10	—	15	—	10	—	15	—	10	—	nS

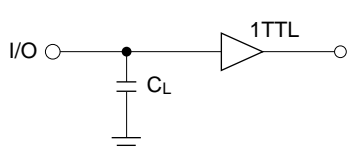
o Write Cycle

V_{SS} = 0V, T_a = -25 to 85°C

Parameter	Symbol	Condi-tions	SRM2B256SLMX55				SRM2B256SLMX70				SRM2B256SLMX10				Unit
			V _{DD} = 3V ±10%		V _{DD} = 5V ±10%		V _{DD} = 3V ±10%		V _{DD} = 5V ±10%		V _{DD} = 3V ±10%		V _{DD} = 5V ±10%		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	*1	100	—	55	—	120	—	70	—	180	—	100	—	nS
Chip Select time	t _{CW}		80	—	50	—	90	—	60	—	110	—	80	—	nS
Address valid to end of write	t _{AW}		80	—	50	—	90	—	60	—	110	—	80	—	nS
Address setup time	t _{AS}		0	—	0	—	0	—	0	—	0	—	0	—	nS
Write pulse width	t _{WP}		75	—	40	—	80	—	45	—	100	—	60	—	nS
Address hold time	t _{WR}		0	—	0	—	0	—	0	—	0	—	0	—	nS
Input data set time	t _{DW}		40	—	25	—	45	—	30	—	60	—	40	—	nS
Input data hold time	t _{DH}		0	—	0	—	0	—	0	—	0	—	0	—	nS
Write to output floating	t _{WHZ}	*2	—	35	—	20	—	40	—	25	—	50	—	35	nS
Output active from end to write	t _{OW}		5	—	5	—	5	—	5	—	5	—	5	—	nS

***1. Test Conditions**

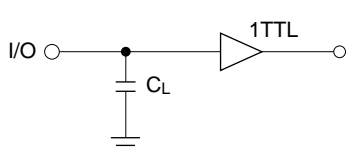
1. Input pulse level: 0.6V to 2.4V (5V) /0.4V to 2.2V (3V)
2. tr = tr = 5ns
3. Input and output timing reference levels : 1.5V
4. Output load C_L = 100pF



C_L = 100pF (Includes Jig Capacitance)

***2. Test Conditions**

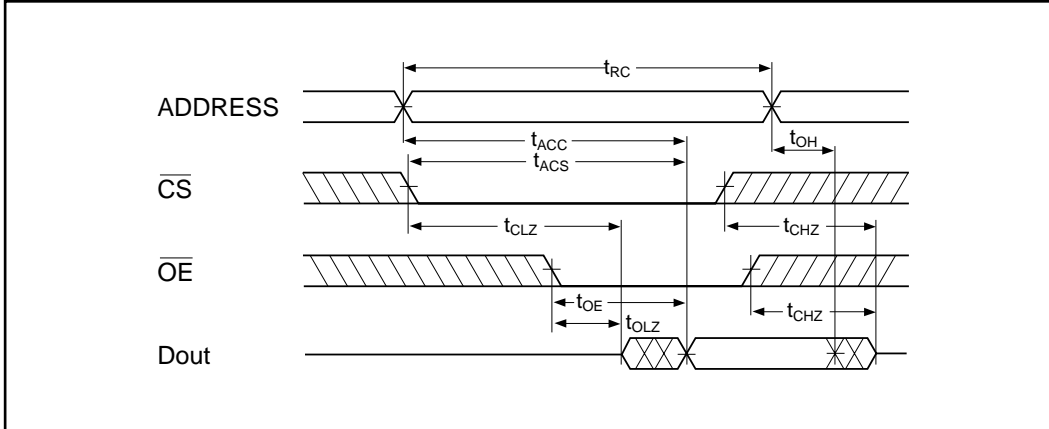
1. Input pulse level: 0.6V to 2.4V (5V) /0.4V to 2.2V (3V)
2. tr = tr = 5ns
3. Input timing reference levels : 1.5V
4. Output timing reference levels: ± 200mV (the level displaced from stable output voltage level)
5. Output load C_L = 5pF



C_L = 5pF (Includes Jig Capacitance)

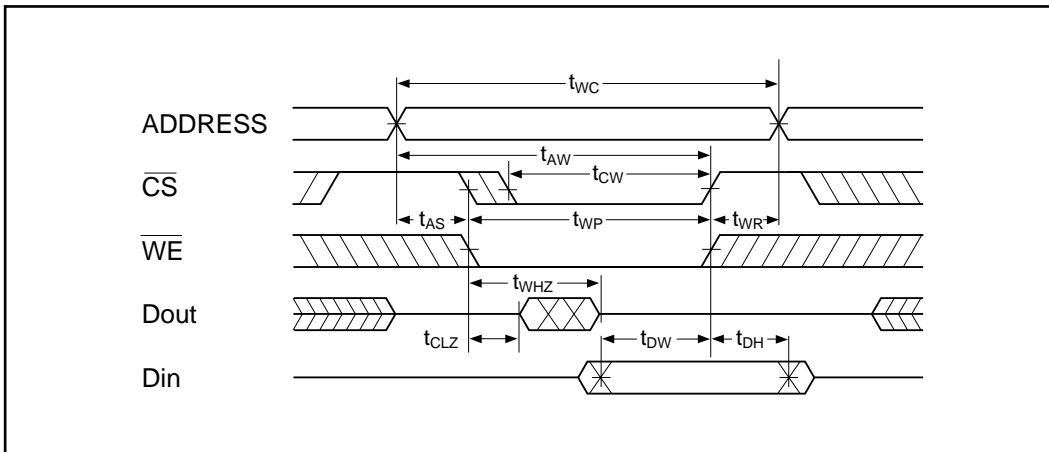
■ Timing Charts

● Read Cycle*1



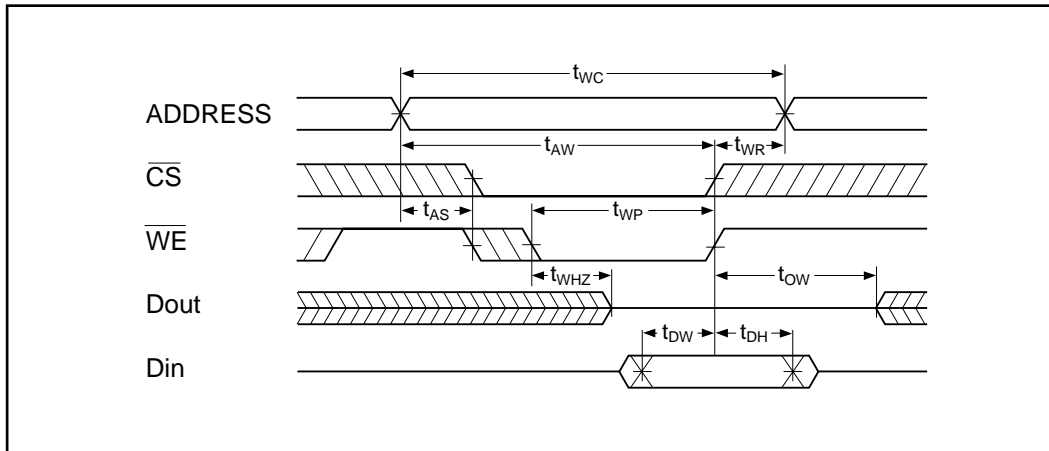
Note: *1. During read cycle time, \overline{WE} must be "H" level.

● Write Cycle (1) (\overline{CS} Control)*2



Note: *2. During write cycle that is controlled by \overline{CS} , Output Buffer is in high impedance state, whether \overline{OE} level is "H" or "L".

● Write Cycle (2) (\overline{WE} Control)*3



Note: *3. During write cycle that is controlled by \overline{WE} , Output Buffer is in high impedance state if \overline{OE} is "H" level.

■ **DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY**

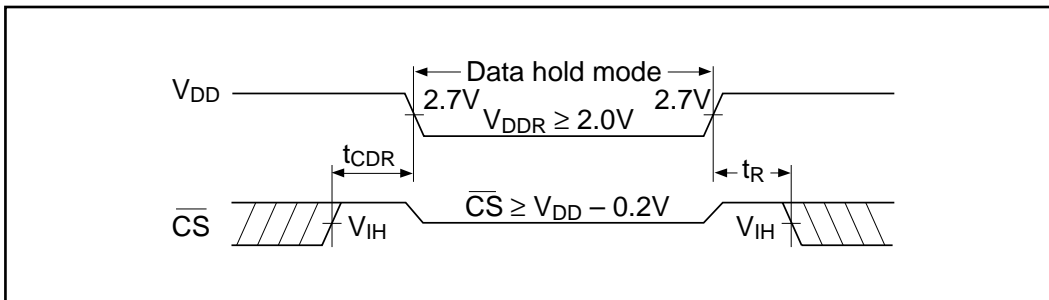
(V_{SS} = 0V, T_a = -25 to 85°C)

Parameter	Symbol	Conditions	Min	Typ*	Max	Unit
Data retention supply voltage	V _{DDR}		2.0	—	5.5	V
Data retention current	I _{DDR}	V _{DD} = 3V CS ≥ V _{DD} - 0.2V	—	0.25	20 (2**)	μA
Chip select data hold time	t _{CDR}		0	—	—	ns
Operation recovery time	t _R		5	—	—	ns

* Typical values are measured at 25°C

** Typical values are measured at 40°C

● **Data Retention Timing**



*Note: During standby mode in which the data is retentive, the supply voltage (V_{DD}) can be in low voltage until V_{DD} = V_{DDR}. At this mode, data reading and writing are impossible.

■ FUNCTIONS

● Truth Table

\overline{CS}	\overline{OE}	\overline{WE}	A0 to A14	Data I/O	Mode	I _{DD}
H	X	X	—	Hi-Z	Standby	I _{DDS} , I _{DDS1}
L	X	L	Stable	D _{IN}	Write	I _{DDA} , I _{DDA1}
L	L	H	Stable	D _{OUT}	Read	I _{DDA} , I _{DDA1}
L	H	H	Stable	Hi-Z	Output disable	I _{DDA} , I _{DDA1}

X: "H" or "L"

—: "H", "L", or "Hi-Z"

● Read Mode

The data appear when the address is set while holding $\overline{CS} = "L"$, $\overline{OE} = "L"$ and $\overline{WE} = "H"$. When $\overline{OE} = "H"$, DATA I/O terminals are in high impedance state, that makes circuit design and bus control easy.

● Write Mode

There are the following 3 ways of writing data into memory:

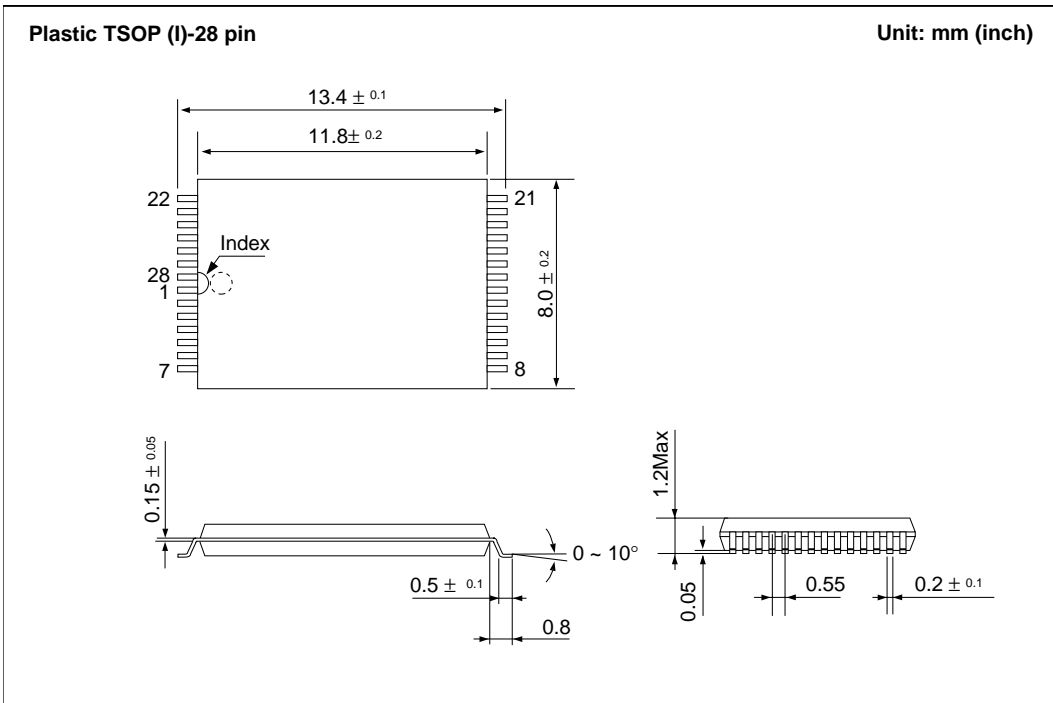
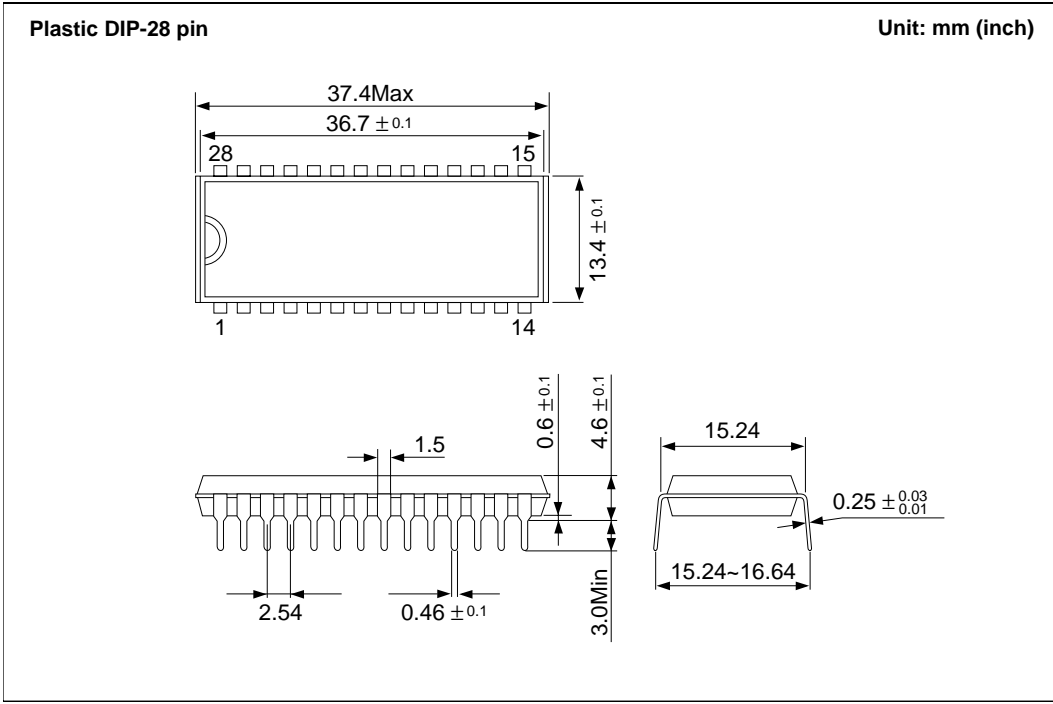
- (1) Hold $\overline{CS} = "L"$ and $\overline{WE} = "L"$, set address
- (2) Hold $\overline{CS} = "L"$ then set address and give "L" pulse to \overline{WE} .
- (3) After setting addresses, give "L" pulse to both \overline{CS} and \overline{WE} .

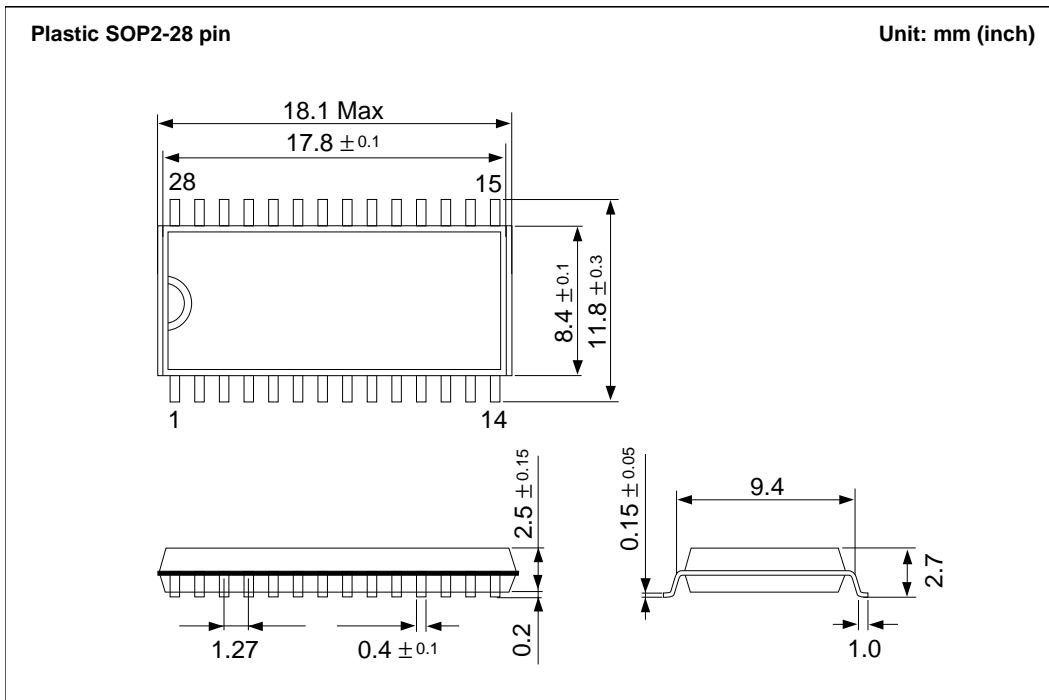
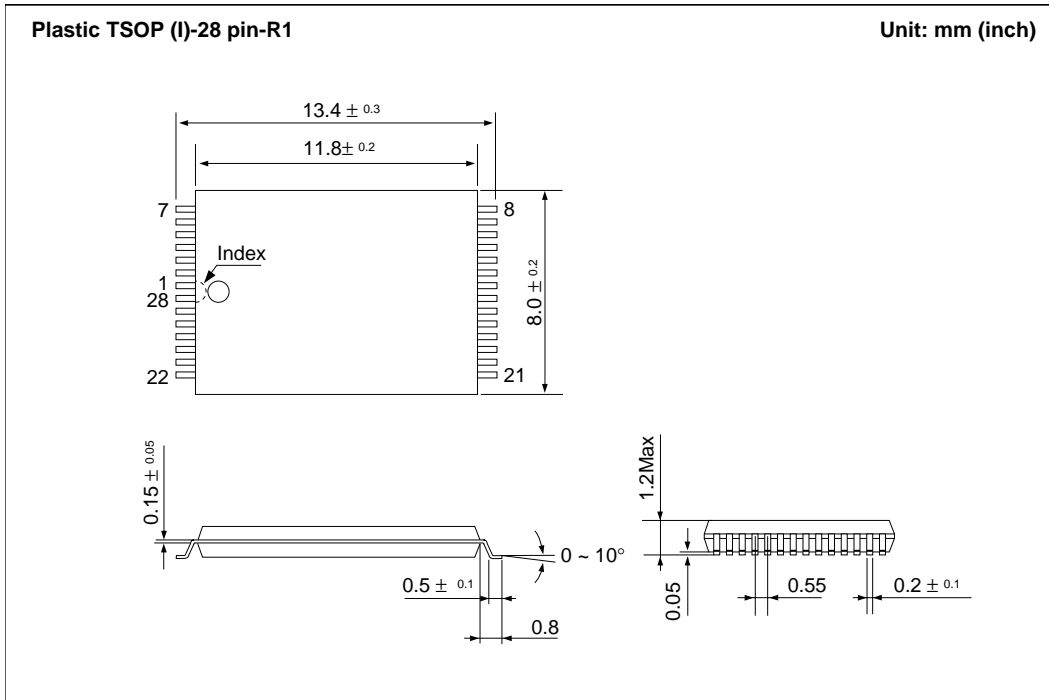
In case the above data on the DATA I/O terminals is latched up into the chip when \overline{CS} or \overline{WE} is in positive-going. Since DATA I/O terminals are high impedance when \overline{CS} or $\overline{OE} = "H"$, bus contention between data driver and memory outputs can be avoided.

● Standby Mode

When \overline{CS} is "H", the chip is in the standby mode. In this mode, DATA I/O terminals are high impedance and all inputs of addresses, \overline{WE} and data can be any "H" or "L". When \overline{CS} is over $V_{DD}-0.2V$, the chip is in the data retention battery backup mode. In this case, there is a small current in the chip which flows through the high resistances of the memory cells.

■ PACKAGE DIMENSIONS





■ CHARACTERISTIC CURVES

