Ideal Diode Bridge Controller

FEATURES

- **Maximizes Power Efficiency**
- **Eliminates Thermal Design Problems**
- **DC to 600Hz**
- **9V to 72V Operating Voltage Range**
- **I_Q = 1.5mA (Typical)**
- Maximizes Available Voltage
- Available in 8-Lead (3mm × 3mm) DFN and 12-Lead MSOP Packages

APPLICATIONS

- Security Cameras
- Terrestrial or Airborne Power Distribution Systems
- Power-over-Ethernet Powered Device with a Secondary Input
- Polarity-Agnostic Power Input
- Diode Bridge Replacement

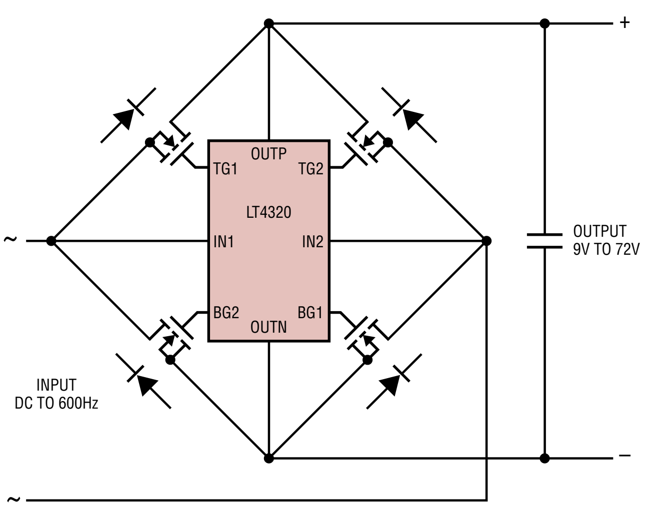
DESCRIPTION

The LT®4320/LT4320-1 are ideal diode bridge controllers that drive four N-channel MOSFETs, supporting voltage rectification from DC to 600Hz. By maximizing available voltage and reducing power dissipation (see thermograph comparison below), the ideal diode bridge simplifies power supply design and reduces power supply cost, especially in low voltage applications.

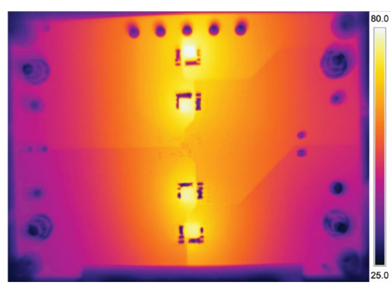
An ideal diode bridge also eliminates thermal design problems, costly heat sinks, and greatly reduces PC board area. The LT4320's internal charge pump supports an all-NMOS design, which eliminates larger and more costly PMOS switches. If the power source fails or is shorted, a fast turn-off minimizes reverse current transients.

The LT4320 is designed for DC to 60Hz voltage rectification, while the LT4320-1 is designed for DC to 600Hz voltage rectification. Higher frequencies of operation are possible depending on MOSFET size and operating load current.

TYPICAL APPLICATION



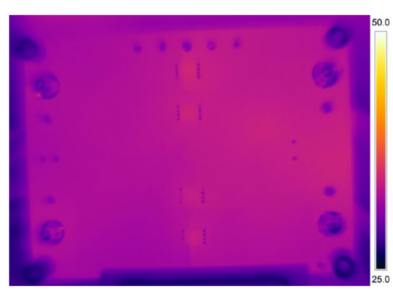
Thermograph of Passive Diode Bridge



SBM1040 (×4)

4320 TA01b

Thermograph of LT4320 Driving Four MOSFETs



LT4320+2.5mΩ FET (×4)

4320 TA01c

CONDITIONS: 24V AC_{IN}, 9.75A DC LOAD ON SAME PCB

Temperature Rise (°C)

CURRENT (A)	MOSFET 2.5mΩ	DIODE SBM 1040
2	0.6	15
4	3.5	32
6	6.7	49
8	11	66
10	16	84

DC Input, On Same PCB

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages
- IN1, IN2 .... –3V to 80V
- OUTP .... –0.3V to 80V

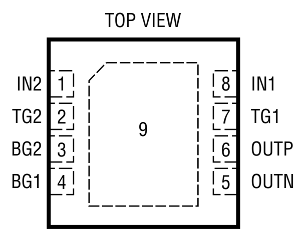
Output Voltages (Note 3)
- BG1, BG2, TG1, TG2 .... –0.3V to 80V
- TG1-IN1, TG2-IN2 .... –0.3V to 12V

Operating Junction Temperature Range
- LT4320I .... –40°C to 85°C

Storage Temperature Range .... –65°C to 150°C

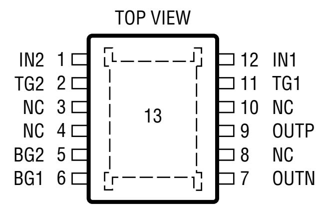
Lead Temperature (Soldering, 10 sec)
- MSE Package .... 300°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 9) MUST BE CONNECTED TO OUTN (PIN 5)



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 13) MUST BE CONNECTED TO OUTN (PIN 7)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	OPERATING JUNCTION TEMPERATURE RANGE
LT4320IDD#PBF	LT4320IDD#TRPBF	LGCV	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT4320IDD-1#PBF	LT4320IDD-1#TRPBF	LGCW	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT4320IMSE#PBF	LT4320IMSE#TRPBF	4320	12-Lead Plastic MSOP	–40°C to 85°C
LT4320IMSE-1#PBF	LT4320IMSE-1#TRPBF	43201	12-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	OUTP Voltage Range		●	9		72	V
	OUTP Undervoltage Lockout (UVLO) Threshold	INn = OUTP, Other IN = 0V	●	6.2	6.6	7.0	V
V_{INT}	INn Turn-On/Off Threshold	OUTP = 9V, Other IN = 0V	●	1.3		3.7	V
I_{OUTP}	OUTP Pin Current	INn = OUTP+ $\Delta V_{SD(MAX)}$ + 5mV, Other IN = 0V	●		1.0	1.5	mA
I_{INn}	INn Pin Current at 9V at 72V	INn = OUTP+ $\Delta V_{SD(MAX)}$ + 5mV, Other IN = 0V	 ● ●		 44 0.3	 63 0.4	 µA mA
ΔV_{SD}	Topside Source-Drain Regulation Voltage (INn – OUTP) LT4320 LT4320-1		 ● ●	 8 26	 20 40	 35 55	 mV mV
ΔV_{TGATE}	Top Gate Drive (TGn – INn)	INn = OUTP+ $\Delta V_{SD(MAX)}$ + 5mV, 10µA Out of TGn, Other IN = 0V	●	6.6		10.8	V
V_{BGATE}	Bottom Gate Drive (BGn)	INn = OUTP, 10µA Out of BGn, Other IN = 0V	●	7.0		12	V
I_{TGUn}	Top Gate Pull-Up Current	TGn – INn = 0V, INn = OUTP + 0.1V TGn – INn = 5V, INn = OUTP + 0.1V Current Flows Out of TGn, Other IN = 0V	● ●	425 120			µA µA
I_{TGSn}	Top Gate Pull-Down Current to INn	TGn – INn = 5V, INn = OUTP – 0.25V Current Flows Into TGn, Other IN = 0V	●	1.25			mA
I_{TGGn}	Top Gate Pull-Down Current to OUTN	INn = 0V, Other IN = OUTP = 9.0V, TGn = 5V Current Flows Into TGn	●	6.0			mA
I_{BGUn}	Bottom Gate Pull-Up Current	BGn = 5V; INn = OUTP = 9.0V, Other IN = 0V Current Flows Out of BGn	●	1.9			mA
I_{BGDn}	Bottom Gate Pull-Down Current	BGn = 5V; INn = 0V, Other IN = OUTP = 9.0V Current Flows Into BGn	●	12.5			mA

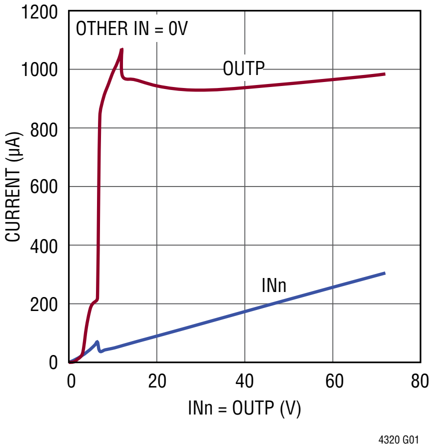
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Unless otherwise specified, exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are referenced to OUTN = 0V unless otherwise specified.

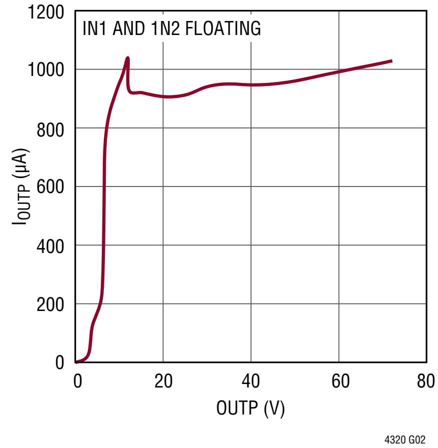
Note 3: Externally forced voltage absolute maximums. The LT4320 may exceed these limits during normal operation.

TYPICAL PERFORMANCE CHARACTERISTICS

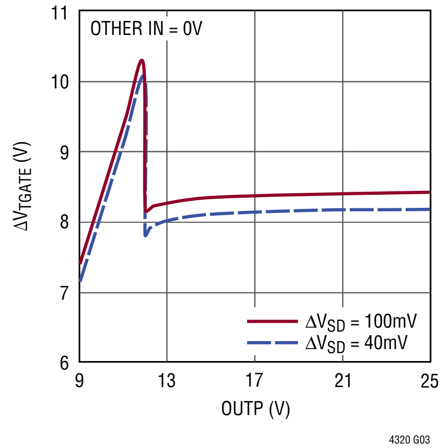
I_{INn} and I_{OUTP} vs OUTP



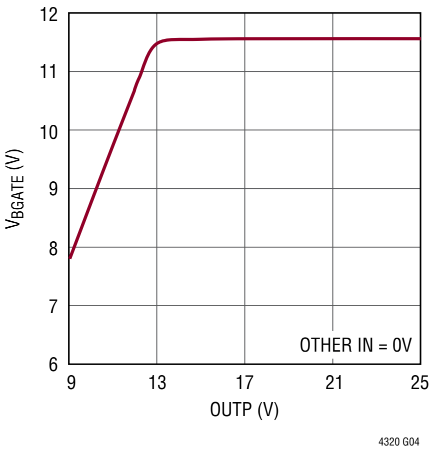
I_{OUTP} vs OUTP



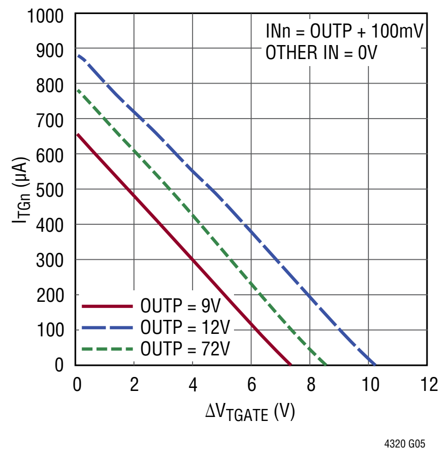
ΔV_{TGATE} vs OUTP



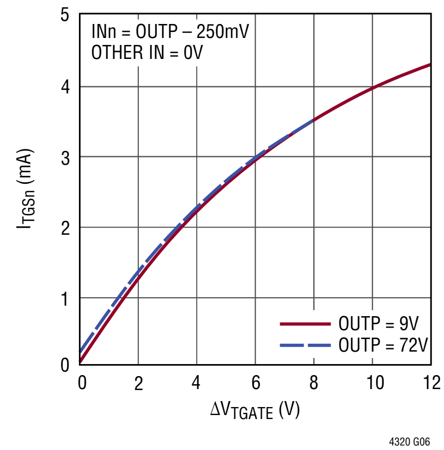
V_{BGATE} vs OUTP



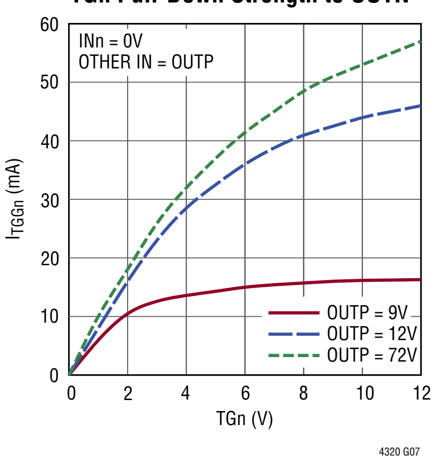
TGn Pull-Up Strength



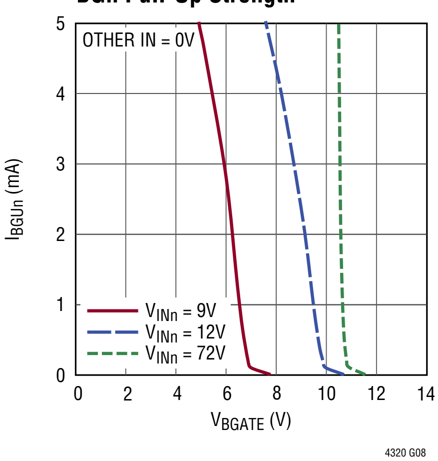
TGn Pull-Down Strength to INn



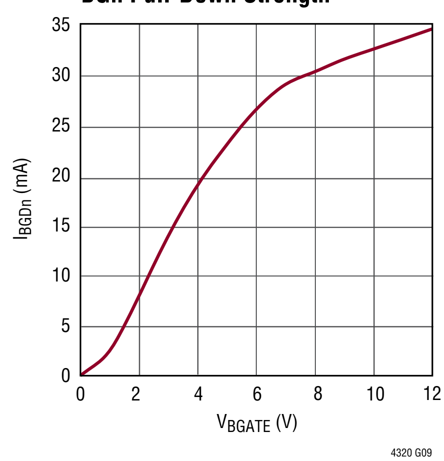
TGn Pull-Down Strength to OUTN



BGn Pull-Up Strength



BGn Pull-Down Strength



PIN FUNCTIONS (DFN/MSOP)

IN2 (Pin 1/Pin 1): Bridge Rectifier Input. IN2 connects to the external NMOS transistors MTG2 source, MBG1 drain and the power input.

TG2 (Pin 2/Pin 2): Topside Gate Driver Output. TG2 pin drives MTG2 gate.

BG2 (Pin 3/Pin 5): Bottom-Side Gate Driver Output. BG2 pin drives MBG2 gate.

BG1 (Pin 4/Pin 6): Bottom-Side Gate Driver Output. BG1 pin drives MBG1 gate.

OUTN (Pin 5/Pin 7): OUTN is the rectified negative output voltage, and connects to the sources of MBG1 and MBG2.

OUTP (Pin 6/Pin 9): OUTP is the rectified positive output voltage that powers the LT4320 and connects to the drains of MTG1 and MTG2.

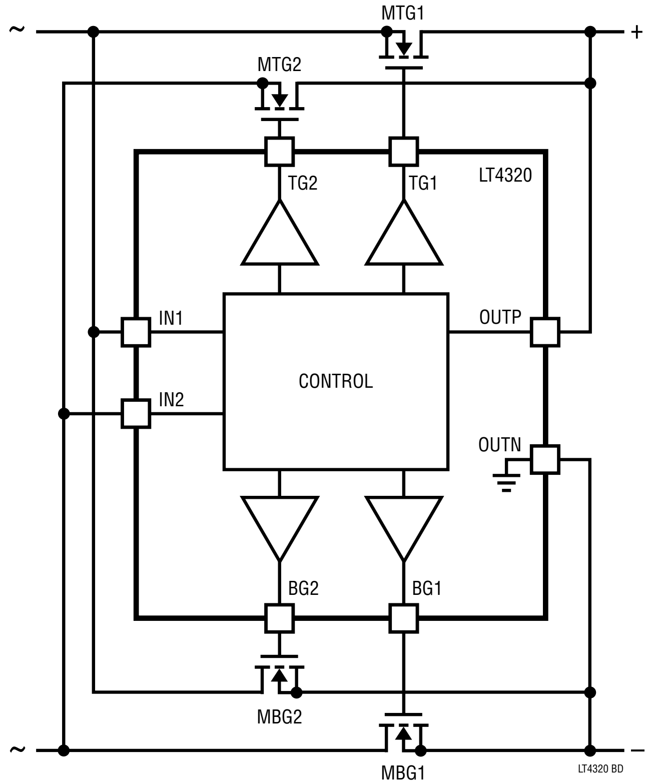
TG1 (Pin 7/Pin 11): Topside Gate Driver Output. TG1 pin drives MTG1 gate.

IN1 (Pin 8/Pin 12): Bridge Rectifier Input. IN1 connects to the external NMOS transistors MTG1 source, MBG2 drain, and the power input.

NC (Pins 3, 4, 8, 10, MSOP Only): No Connections. Not internally connected.

Exposed Pad (Pin 9/Pin 13): Exposed Pad. Must be connected to OUTN.

BLOCK DIAGRAM



OPERATION

Electronic systems that receive power from an AC power source or a DC polarity-agnostic power source often employ a 4-diode rectifier. The traditional diode bridge comes with an efficiency loss due to the voltage drop generated across two conducting diodes. The voltage drop reduces the available supply voltage and dissipates significant power especially in low voltage applications.

By maximizing available voltage and reducing power dissipation, the ideal diode bridge simplifies power supply design and reduces power supply cost. An ideal diode bridge also eliminates thermal design problems, costly heat sinks, and greatly reduces PC board area.

The LT4320 is designed for DC to 60Hz voltage rectification, while the LT4320-1 is designed for DC to 600Hz voltage rectification. Higher frequencies of operation are possible depending on MOSFET size and operating load current.

Figure 2 presents sample waveforms illustrating the gate pins in an AC voltage rectification design.

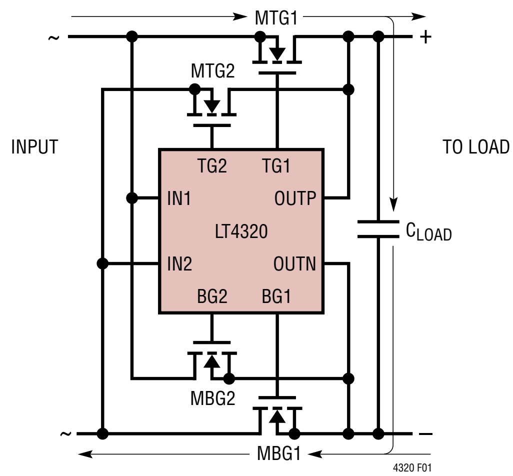


Figure 1. LT4320 with Four N-Channel MOSFETS, Illustrating Current Flow When IN1 Is Positive

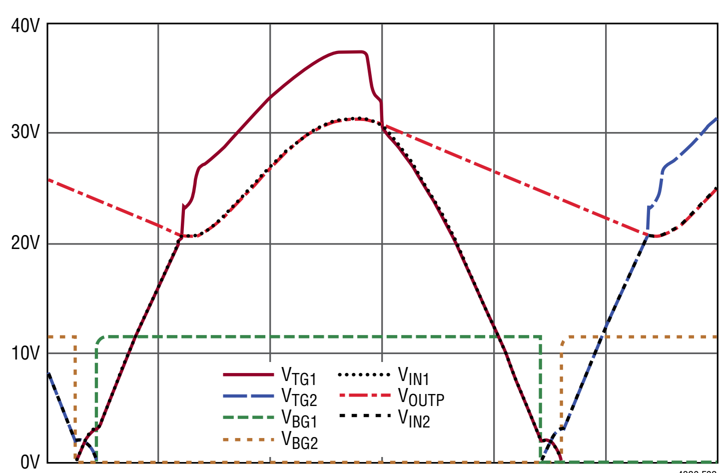


Figure 2. 24V AC Sample Waveform

APPLICATIONS INFORMATION

MOSFET Selection

A good starting point is to reduce the power dissipation of the ideal bridge to 1/10 that of a diode rectifier bridge. Given the average output load current, I_{AVG}, select $R_{DS(ON)}$ to be:

$$R_{DS(ON)} = \frac{70mV}{I_{AVG}} \text{ for a DC power input}$$

or

$$R_{DS(ON)} = \frac{70mV}{3 \cdot I_{AVG}} \text{ for an AC power input}$$

In the AC power input calculation, $3 \cdot I_{AVG}$ assumes the duration of current conduction occupies 1/3 of the AC period.

Select the maximum allowable drain-source voltage, V_{DSS}, to be higher than the maximum input voltage.

Design Example

For a 24W, 12V DC/24V AC application, I_{AVG} = 2A for 12V DC. To cover the 12V DC case:

$$R_{DS(ON)} = \frac{70mV}{2A} = 35m\Omega$$

For the 24V AC operation, I_{AVG} = 1A. To cover the 24V AC case:

$$R_{DS(ON)} = \frac{70mV}{3 \cdot 1A} = 23m\Omega$$

This provides a starting range of $R_{DS(ON)}$ values to choose from.

Ensure the MOSFET can handle a continuous current of $3 \cdot I_{AVG}$ to cover the expected peak currents during AC rectification. That is, select $I_D \geq 3A$. Since a 24V AC waveform can reach 34V peak, select a MOSFET with V_{DSS} >>34V. A good choice of V_{DSS} is 60V in a 24V AC application.

Other Considerations in MOSFET Selection

Choose the lowest available total gate charge, Q_G, and correspondingly the lowest C_{ISS}, C_{OSS}, and C_{RSS}. Choosing a lower gate capacitance while meeting $R_{DS(ON)}$ speeds up the response time for full enhancement, regulation, turn-off, and input shorting events.

$V_{GS(th)}$ must be a minimum of 2V or higher. A gate threshold voltage lower than 2V is not recommended since too much time is needed to discharge the gate below the threshold and halt current conduction during a hot plug or input short event.

C_{LOAD} Selection

A 1µF ceramic and a 10µF minimum electrolytic capacitor must be placed across the OUTP and OUTN pins with the 1µF ceramic placed as close to the LT4320 as possible. Downstream power needs and voltage ripple tolerance determine how much additional capacitance between OUTP and OUTN is required. C_{LOAD} in the hundreds to thousands of microfarads is common.

A good starting point is selecting C_{LOAD} such that:

$$C_{LOAD} \geq I_{AVG}/(V_{RIPPLE} \cdot 2 \cdot Freq)$$

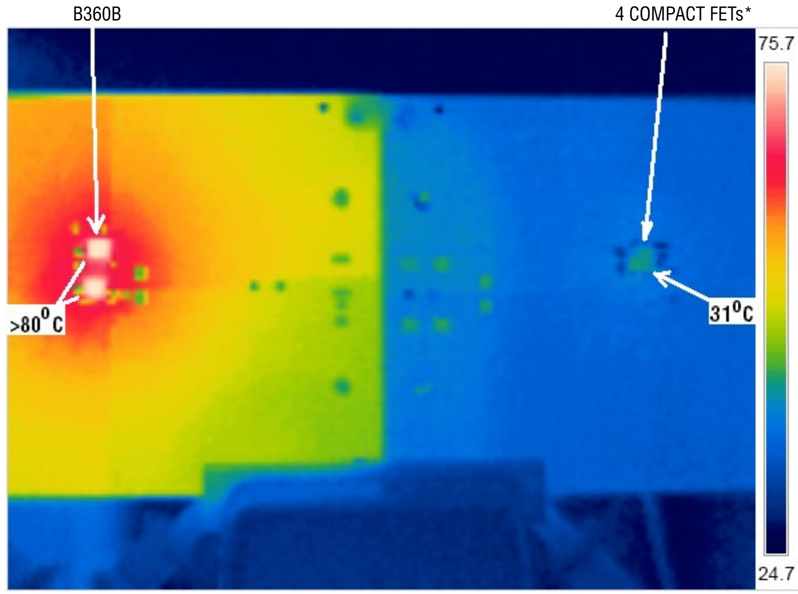
where I_{AVG} is the average output load current, V_{RIPPLE} is the maximum tolerable output ripple voltage, and Freq is the frequency of the input AC source. For example, in a 60Hz, 24VAC application where the load current is 1A and the tolerable ripple is 15V, choose $C_{LOAD} \geq$ 1A/(15V • 2 • 60Hz) = 556µF.

C_{LOAD} must also be selected so that the rectified output voltage, OUTP-OUTN, must be within the LT4320/LT4320-1 specified OUTP voltage range.

Transient Voltage Suppressor

For applications that may encounter brief overvoltage events higher than the LT4320 absolute maximum rating, install a unidirectional transient voltage suppressor (TVS) between the OUTP and OUTN pins as close as possible to the LT4320.

TYPICAL APPLICATIONS



CONDITION: 13VDC$_{IN}$, 3A LOAD ON SAME PCB

*19mΩ, 60V EACH FET

Figure 3. Thermograph: B360B vs LT4320 +4 Compact FETs

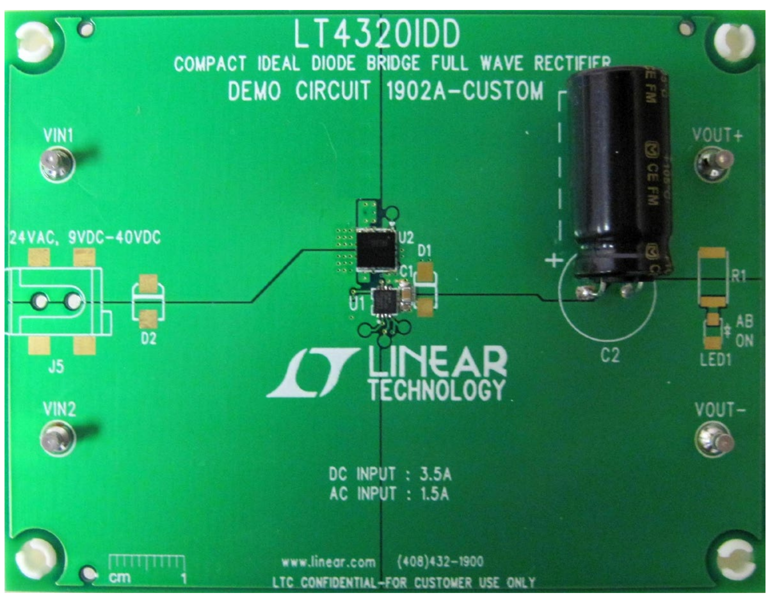
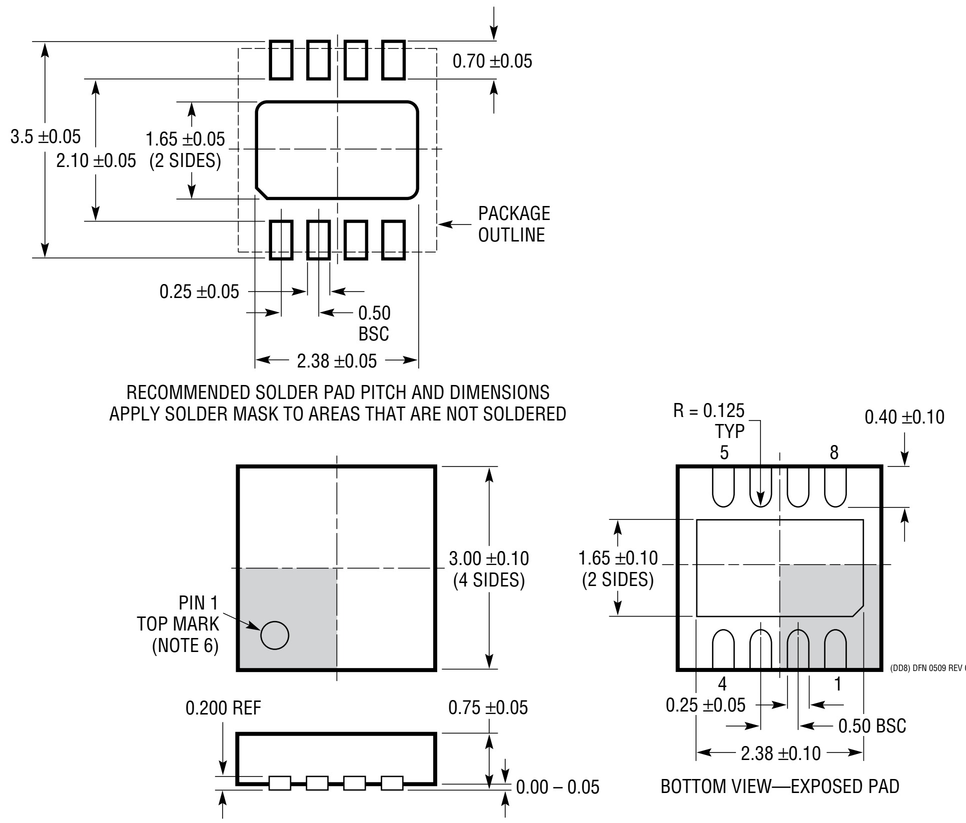


Figure 4. Demonstration Circuit 1902A Used in Figure 3 Thermograph

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)

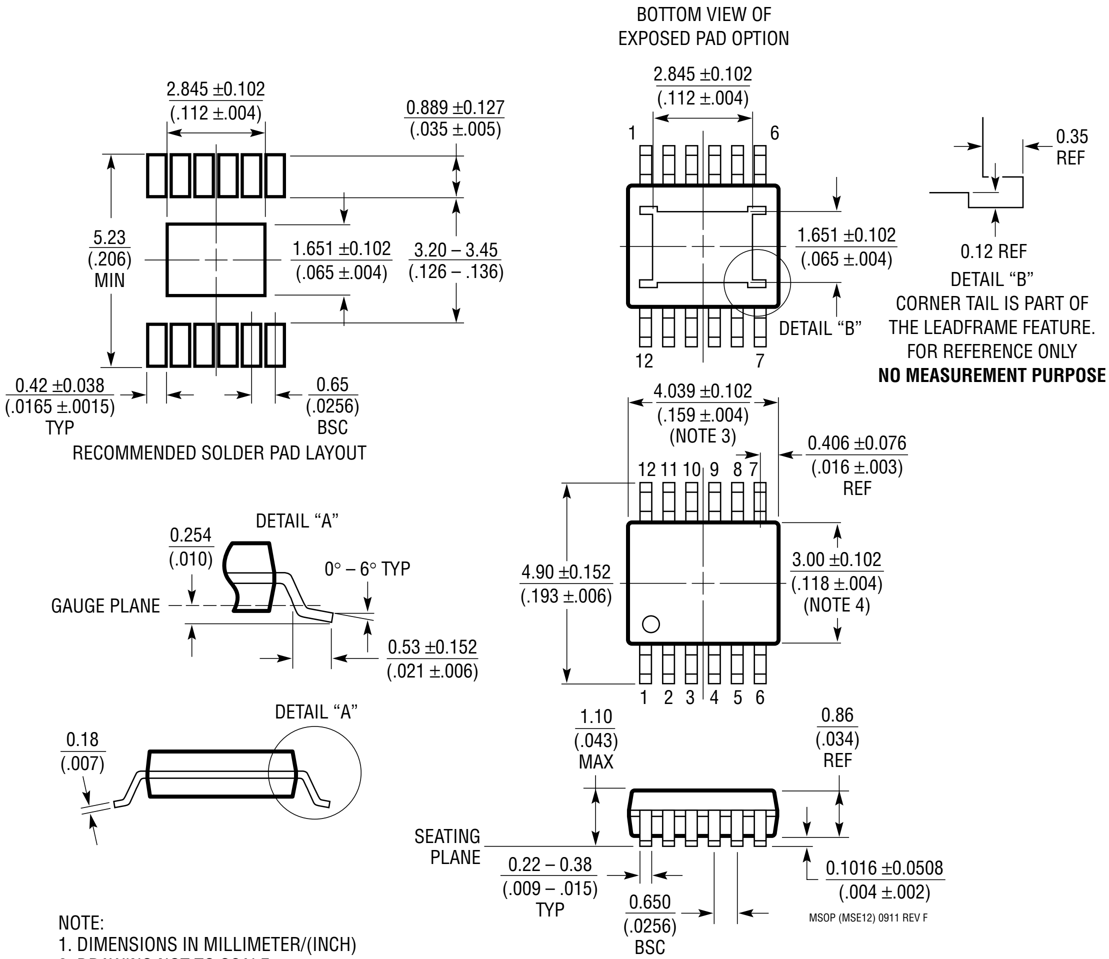


NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

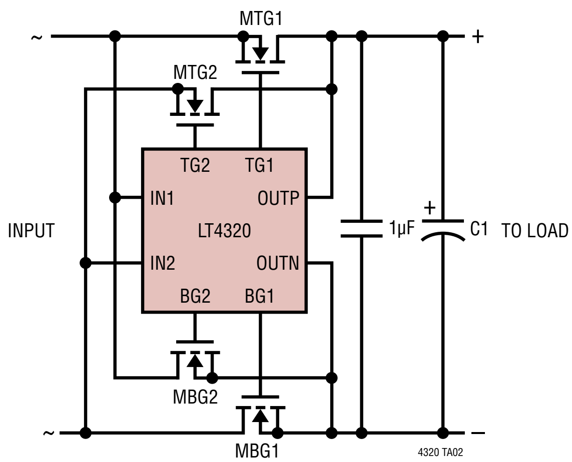
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION



LT4320 IDEAL BRIDGE					DIODE BRIDGE
MTG1, MTG2 MBG1, MBG2	OPERATING VOLTAGE	LOAD CURRENT	C1 (MIN)	POWER LOSS	POWER LOSS
BSZ110N06NS3	55V DC	3.5A	10µF	0.22W	4.2W
	24V AC	1.5A	560µF	0.13W	1.9W
BSC031N06NS3	55V DC	30A	10µF	4.5W	36W
	24V AC	10A	3.3mF	1.6W	12W
PSMN040-100MSE	72V DC	2A	10µF	0.24W	2.4W

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4352	Low Voltage Ideal Diode Controller with Monitoring	N-Channel, 0V to 18V, UV, OV, MSOP-12 and DFN-12 Packages
LTC4353	Dual Low Voltage Ideal Diode Controller	Dual N-Channel, 0V to 18V, MSOP-16 and DFN-16 Packages
LTC4354	Negative Voltage Diode-OR Controller and Monitor	Controls Two N-Channel MOSFETs, 1µs Turn-Off, –80V Operation
LTC4355	Positive Voltage Diode-OR Controller and Monitor	Controls Two N-Channel MOSFETs, 0.5µs Turn-Off, 9V to 80V Operation
LTC4357	Positive High Voltage Ideal Diode Controller	Controls Single N-Channel MOSFETs, 0.5µs Turn-Off, 9V to 80V Operation
LTC4358	5A Ideal Diode	Positive Voltage Ideal Diode with Integrated MOSFET, 9V to 26.5V Operation
LTC4359	Ideal Diode Controller with Reverse Input Protection	N-Channel, 4V to 80V, MSOP-8 and DFN-6 Packages
LTC4370	2-Supply Diode-OR Current Balancing Controller	Dual N-Channel, 0V to 18V, MSOP-16 and DFN-16 Packages
LTC4415	Dual 4A ideal Diodes with Adjustable Current Limit	1.7V to 5.5V Operating Range

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