参考資料

HM678127UH Series

131,072-word × 8-bit High Speed CMOS Static RAM

HITACHI

Features

- 131,072-word × 8-bit organization
- Directly TTL compatible input and output
- Choice of 5.0 V or 3.3 V power supplies for output buffers
- Completely static memory
- No clock or timing strobe required
- Super fast access time: 10/12 ns (max)
- Revolutional pin arrangement

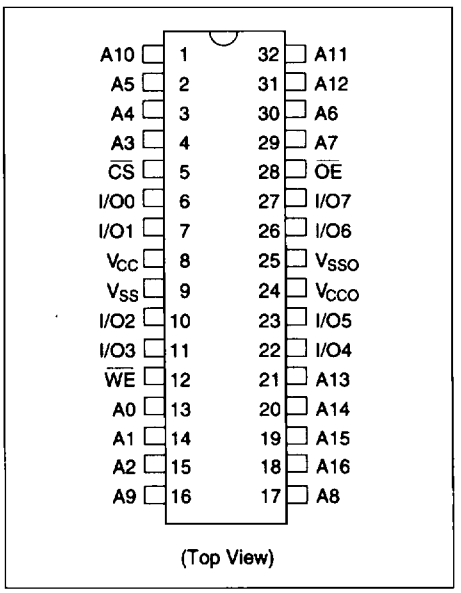
Ordering Information

Type No.	Access time	Package
HM678127UHJ-10	10 ns	400 mil 32 pin Plastic SOJ (CP-32DB)
HM678127UHJ-12	12 ns	

Pin Description

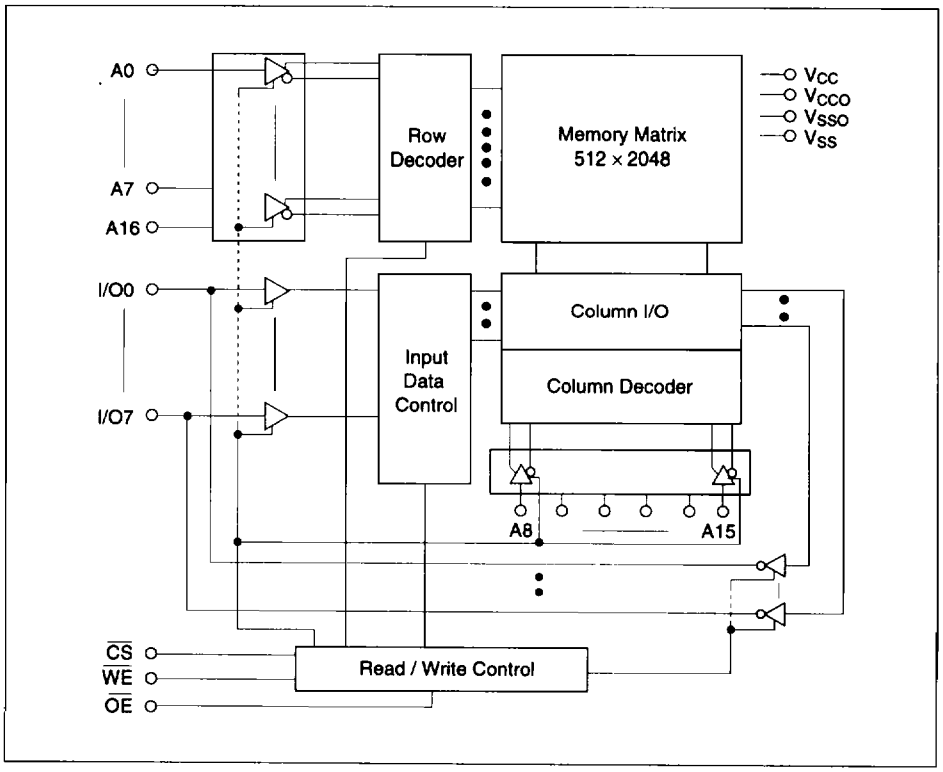
Pin name	Function
A0 – A16	Address input
I/O0 – I/O7	Data input/output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
V_{CC}	+5 V power supply
V_{CCO}	Output buffer power supply
V_{SSO}	Output buffer ground
V_{SS}	Ground

Pin Arrangement



(Top View)

Block Diagram



Function Table

Input

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Output	Mode	V_{CC} current	Reference cycle
H	X	X	High-Z	Not selected	I_{SB}, I_{SB1}	—
L	H	H	High-Z	Output disable	I_{CC}, I_{CC1}	—
L	H	L	Data out	Read	I_{CC}, I_{CC1}	Read cycle 1, 2, 3
L	L	H	Data in	Write	I_{CC}, I_{CC1}	Write cycle 1, 2, 3, 4
L	L	L	Data in	Write	I_{CC}, I_{CC1}	Write cycle 5, 6

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}*1	V_T	–0.5 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0*2, 1.3*3	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg(bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to $V_{SS} = V_{SSO}$
2. Under the transverse air flow < 500 linear feet/minute
3. Under the transverse air flow ≥ 500 linear feet/minute

For the DC and AC specifications shown in these tables, this device was tested under a minimum transverse air flow exceeding 500 linear feet per minute.

Recommended DC Operating Conditions ($0°C \leq Ta \leq +70°C$)

Parameter		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.5	5.0	5.5	V
	5 V TTL compatible	V_{CCQ}	4.5	5.0	5.5	V
	3.3 V TTL compatible		3.0	3.3	3.6	V
		V_{SS}, V_{SSQ}	0.0	0.0	0.0	V
Input high voltage		V_{IH}	2.2	—	V_{CC} + 0.5	V
Input low voltage		V_{IL}	–0.5	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{CCO} = 5.0 V ± 10 % or 3.3 V ± 0.3 V, V_{SS} = V_{SSO} = 0 V, Ta = 0 to +70°C)

		HM678127UH					
		-10		-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Input leakage current	$\|I_{LI}\|$	—	2	—	2	µA	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	10	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 V to V_{CCO}
Operating power supply current	I_{CC}	—	120	—	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	200	—	190	mA	Min. cycle, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	45	—	45	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	—	35	—	35	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	2.4	—	V	I_{OH} = –4 mA

Capacitance (Ta =25°C, f=1 MHz)

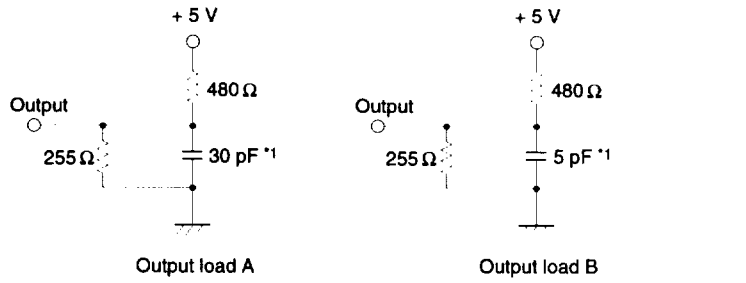
Parameter	**Symbol**	**Max**	**Unit**	**Test condition**
Input capacitance	C_{IN}*1	6	pF	V_{IN} = 0 V
Input/output capacitance	$C_{I/O}$*1	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and has not been 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{CCO} = 5.0 V ± 10 % or 3.3 V ± 0.3 V, V_{SS} = V_{SSO} = 0 V, Ta = 0 to +70°C, unless otherwise noted)

Test conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels: 1.5 V
- Output load: See figure
- Input rise and fall time: 4 ns
- Output reference level: 1.5 V



Note: 1. including scope and jig capacitance

Read Cycle

		HM678127UH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	10	—	12	—	ns
Address access time	t_{AA}	—	10	—	12	ns
Chip select access time	t_{ACS}	—	10	—	12	ns
Chip selection to output in low-Z	t_{LZ}*1, *2	3	—	4	—	ns
Output enable to output valid	t_{OE}	—	5	—	6	ns
Output enable to output in low-Z	t_{OLZ}*1, *2	0	—	0	—	ns
Chip deselection to output in high-Z	t_{HZ}*1, *2	0	5	0	6	ns
Output hold from address change	t_{OH}	3	—	4	—	ns

Notes: 1. This parameter is sampled and has not been 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

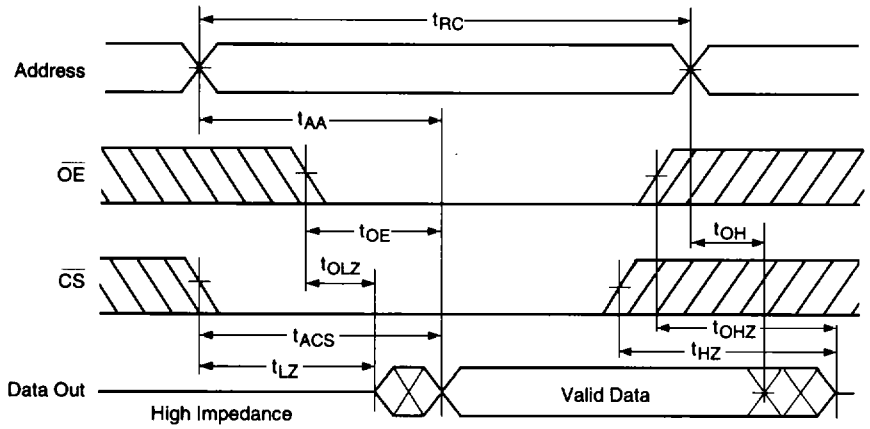
Write Cycle

		HM678127UH				
		-10		-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}*1	10	–	12	–	ns
Chip selection to end of write	t_{CW}	8	–	10	–	ns
Address valid to end of write	t_{AW}	8	–	10	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	8	–	10	–	ns
Write recovery time	t_{WR}	0	–	0	–	ns
Data valid to end of write	t_{DW}	5	–	6	–	ns
Data hold time	t_{DH}	0	–	0	–	ns
Write enable to output in high-Z	t_{WZ}*2, *3	0	5	0	6	ns
Output disable to output in high-Z	t_{OHZ}*2, *3	0	5	0	6	ns
Output active from end of write	t_{OW}*2, *3	0	–	0	–	ns

Notes: 1. All write cycle timings are referred from the last valid address to the first transitioning address.
2. This parameter is sampled and has not been 100% tested.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

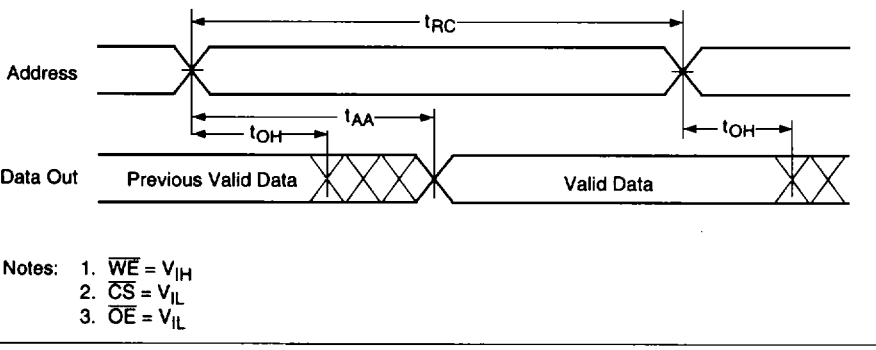
Timing Waveforms

Read Cycle 1



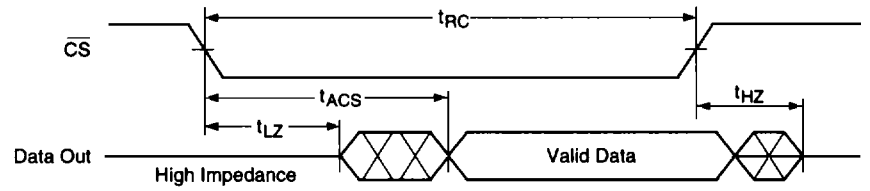
Note: 1. $\overline{WE} = V_{IH}$

Read Cycle 2



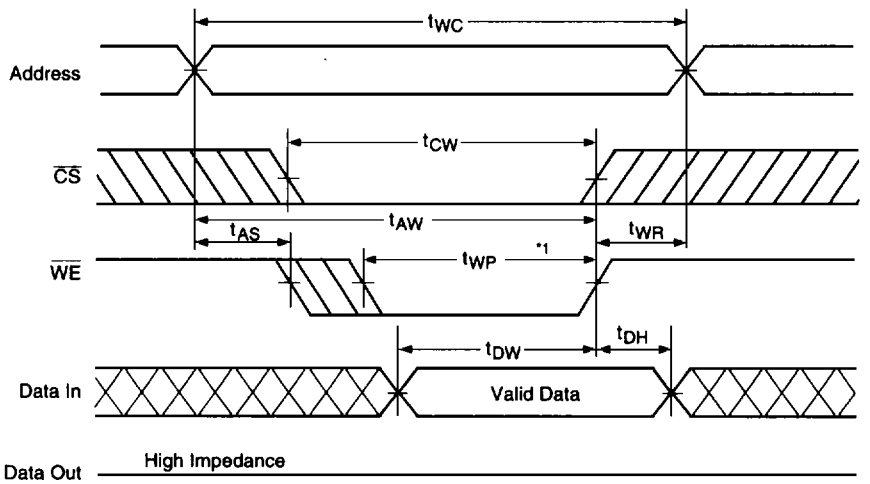
Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

Read Cycle 3

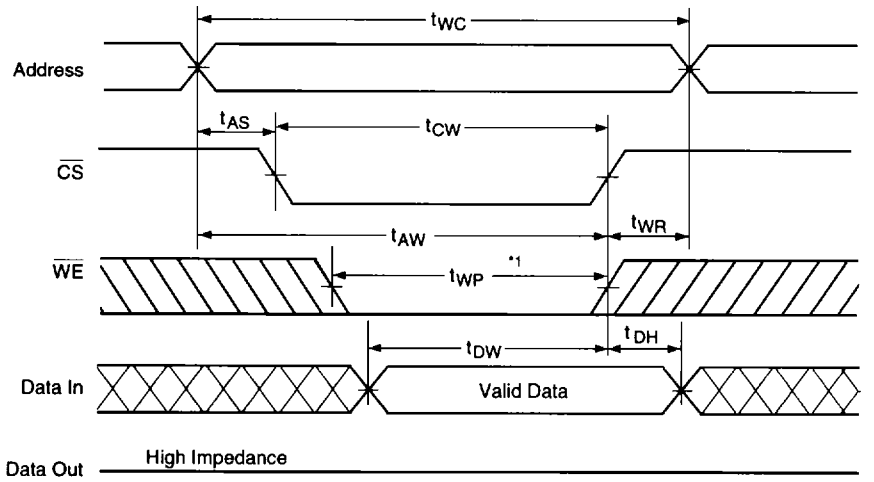


Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{OE} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle 1 ($\overline{OE}$ = H, $\overline{WE}$ Controlled)

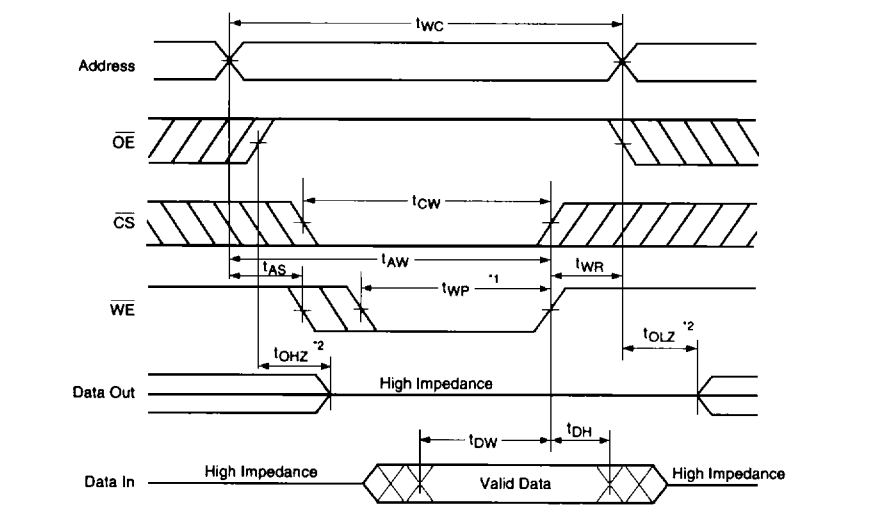


Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).



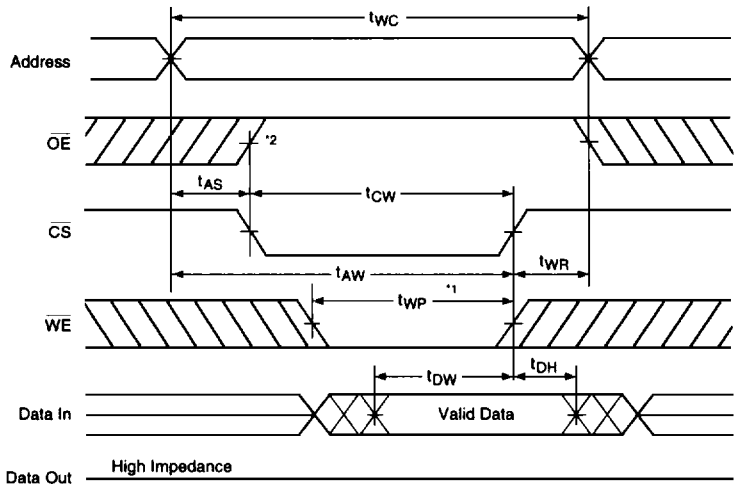
Note: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).

Write Cycle 2 ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



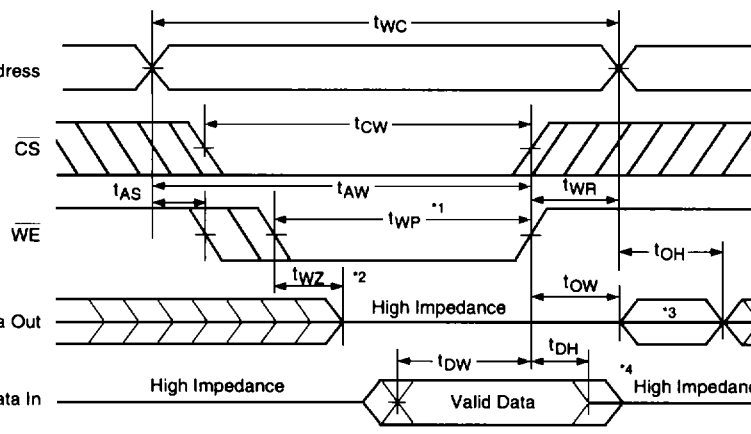
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

Write Cycle 3 ($\overline{OE}$ = clocked, $\overline{WE}$ controlled)



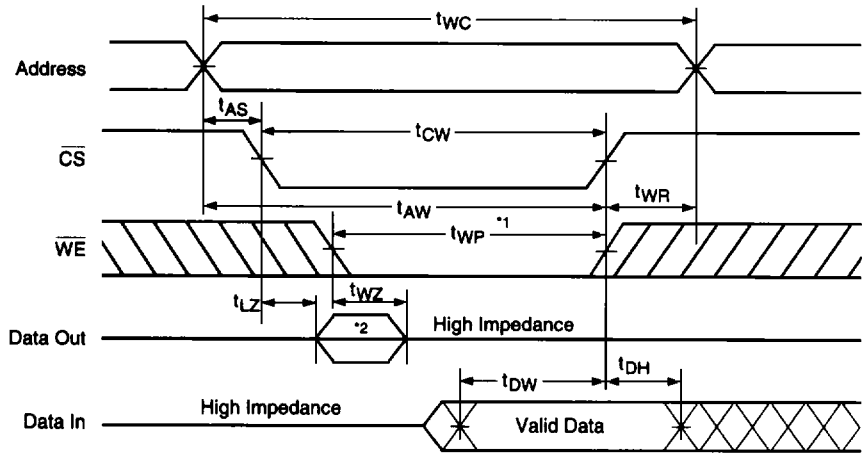
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in a high impedance state.

Write Cycle 4 ($\overline{OE}$ = clocked, CS controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

Write Cycle 5 ($\overline{OE}$ = L, $\overline{WE}$ controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

Write Cycle 6 ($\overline{OE}$ = L, CS controlled)