

# M81049P/SP/FP

OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

## DESCRIPTION

M81049 is octal D-type flip-flop driver by 20-pin package. It has 8 same circuit units which is composed of D-type flip-flop logic circuit and high voltage NchMOS output transistor. M81049 has a common direct clear input and a common clock input.

## FEATURES

- Lineup with three packages
- High breakdown voltage ( $BV_{DSX} \geq 40V$ )
- Drain output current ( $I_{DS(max)} = 200mA$ )
- With input protection diodes
- Pin assignment of input-output flow through
- Wide operating temperature range ( $T_a = -40$  to  $+85^\circ C$ )

## APPLICATION

LED drive

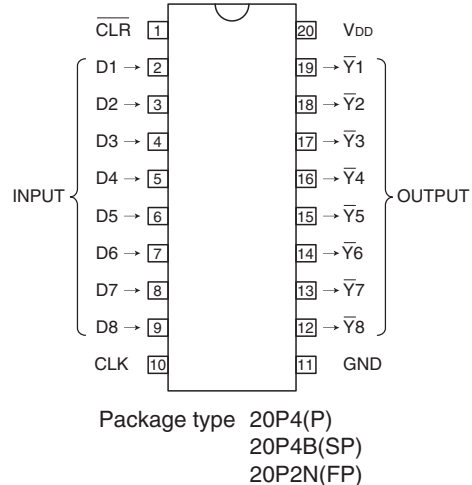
## FUNCTION

The common direct clear input and common clock input are connected to every circuit unit by the same way. Signal at the D inputs is transferred to  $\bar{Y}$  outputs by D-type flip-flops on the positive-going edge of the clock pulse.

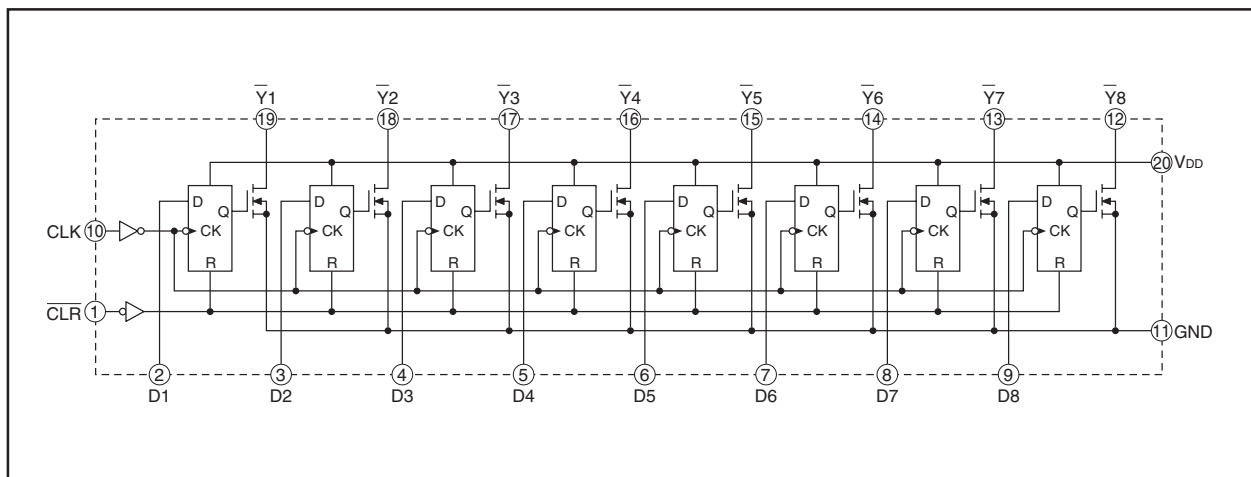
If  $\overline{CLR}$  is set to "L", outputs  $\bar{Y}1$ - $\bar{Y}8$  will be altogether set to "H" regardless of D1-D8 and CLK.

The maximum drain current of an output is 200mA. The maximum between drain-source is 40V.

## PIN CONFIGURATION (TOP VIEW)



## LOGIC DIAGRAM (POSITIVE LOGIC)



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**FUNCTION TABLE (EACH CHANNEL)**

INPUT			OUTPUT : $\bar{Y}$
CLR	CLK	D	
L	X	X	H
H	↑	L	H
H	↑	H	L
H	L	X	Latched
H	↓	X	Latched

↑ : "L" to "H"

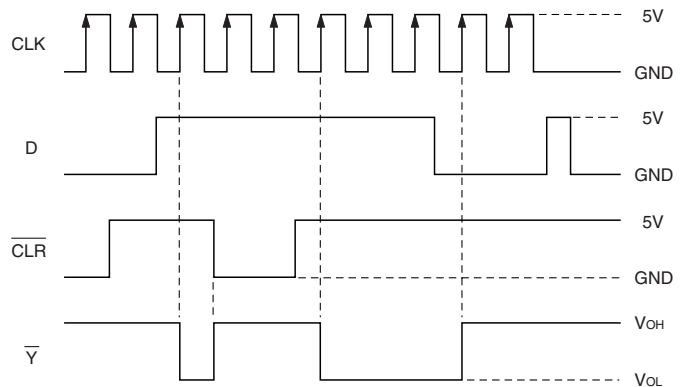
↓ : "H" to "L"

H : High level

L : Low level

X : Irrelevant

**TIMING DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, Ta = -40 ~ +85°C)**

Symbol	Parameter	Conditions	Ratings	Unit	
VDD	Supply voltage		7	V	
VDS	Drain-to-source voltage	Output, H	-0.5 ~ +40	V	
VI	Input voltage		-0.5 ~ VDD	V	
IDS	Drain output current	Current per circuit output, L	200	mA	
Pd	Power dissipation	Ta = 25°C, when mounted on board	M81049P	1.79	W
			M81049SP	1.47	
			M81049FP	1.10	
Topr	Operating temperature		-40 ~ +85	°C	
Tstg	Storage temperature		-55 ~ +125	°C	

**RECOMMENDED OPERATING CONDITIONS (Unless otherwise noted, Ta = -40 ~ +85°C)**

Symbol	Parameter	Conditions	Limits			Unit	
			min	typ	max		
VDD	Supply voltage		4.5	5.0	5.5	V	
VDS	Drain-to-source voltage		0	—	40	V	
VIH	"H" input voltage		0.7VDD	—	VDD	V	
VIL	"L" input voltage		0	—	0.3VDD	V	
IDS	Drain output current (Current per 1 circuit when 8 circuits are coming on simultaneously)	P	Duty Cycle no more than 48%	0	—	200	mA
			Duty Cycle no more than 100%	0	—	140	
		SP	Duty Cycle no more than 40%	0	—	200	
			Duty Cycle no more than 100%	0	—	125	
		FP	Duty Cycle no more than 33%	0	—	200	
			Duty Cycle no more than 100%	0	—	115	
VIN	Input voltage		0	—	VDD	V	
tr,tf	Rise time, Fall time, drain output	VDD = 4.5V	0	—	500	ns	
tsu	Setup time before CLK ↑	VDD = 4.5V	20	—	—	ns	
th	Hold time, data after CLK ↑	VDD = 4.5V	5	—	—	ns	
tw	Pulse duration	VDD = 4.5V	40	—	—	ns	
f	Clock frequency	VDD = 4.5V	—	—	20	MHz	

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### ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $V_{DD} = 5V$ , $T_a = 25^\circ C$ )

Symbol	Parameter	Test conditions	Limits			Unit	
			min	typ	max		
$V_{(BR)DSX}$	Drain-source breakdown voltage	$I_{DS} = 1mA$	40	—	—	V	
$I_{DSX}$	Drain-source leakage current	$V_{DS} = 40V$	—	0.002	5	$\mu A$	
$I_{IH}$	"H" input current	$V_{DD} = 5.5V, V_i = 5.5V$	—	0.005	1	$\mu A$	
$I_{IL}$	"L" input current	$V_{DD} = 5.5V, V_i = 0V$	—	0.005	-1	$\mu A$	
$I_{CC}$	Supply current	$V_{DD} = 5.5V$ $V_i = 5.5V$ or $0V$	All outputs off	—	0.005	5	$\mu A$
		All outputs on	—	0.005	5		
$V_{DS}$	"L" output voltage	$I_{DS} = 100mA, V_{DD} = 4.5V$	—	0.29	0.44	V	
		$I_{DS} = 200mA, V_{DD} = 4.5V$	—	0.59	0.88		
$R_{DS(on)}$	Drain-source on-state resistance	$I_{DS} = 100mA, V_{DD} = 4.5V$	—	2.9	4.4	$\Omega$	

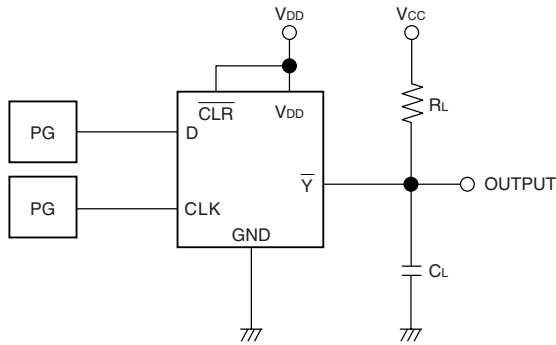
### SWITCHING CHARACTERISTICS ( $V_{DD} = 5V$ , $T_a = 25^\circ C$ )

Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
$t_{TLH}$	Low-level to high-level and high-level to low-level output transition time	$C_L = 30pF$ (Note 1)	—	11	—	ns
$t_{THL}$			—	3	—	ns
$t_{PLH}$	Low-level to high-level and high-level to low-level output propagation time (CLK- $\bar{Y}$ )		—	32	—	ns
$t_{PHL}$			—	26	—	ns
$t_{PLH(R)}$	Low-level to high-level output propagation time (CLR- $\bar{Y}$ )		—	32	—	ns

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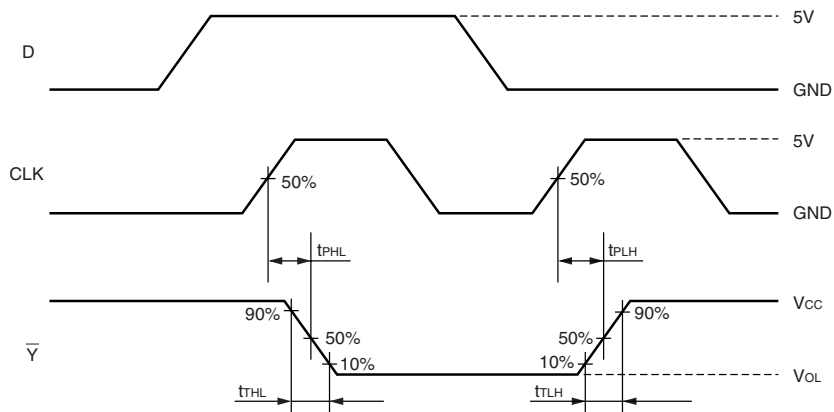
## OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

### NOTE 1 TEST CIRCUIT

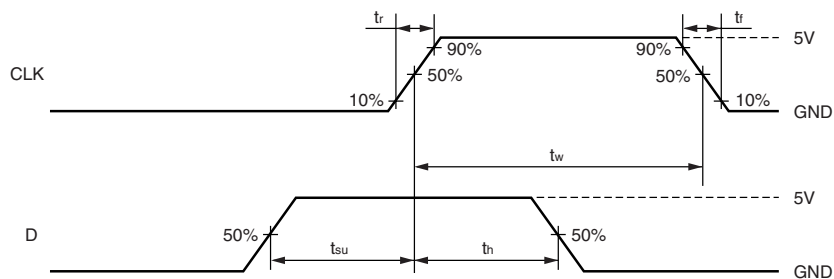


- (1) Pulse generator (PG) characteristics : PRR = 1MHz, Duty Cycle = 50%,  $t_r = 6ns$ ,  $t_f = 6ns$ ,  $Z_o = 50\Omega$ ,  $V_i = 5V$
- (2) Output conditions :  $R_L = 240\Omega$ ,  $V_{CC} = 24V$ ,  $V_{DD} = 5V$
- (3) Electrostatic capacity  $C_L$  includes floating capacitance at connections and input capacitance at probes.

### TIMING DIAGRAM



SWITCHING TIMES

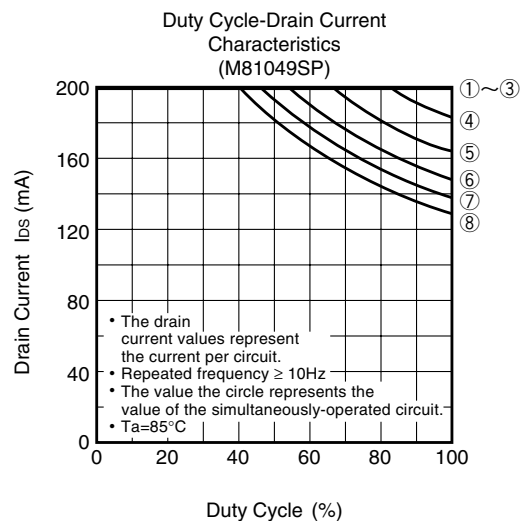
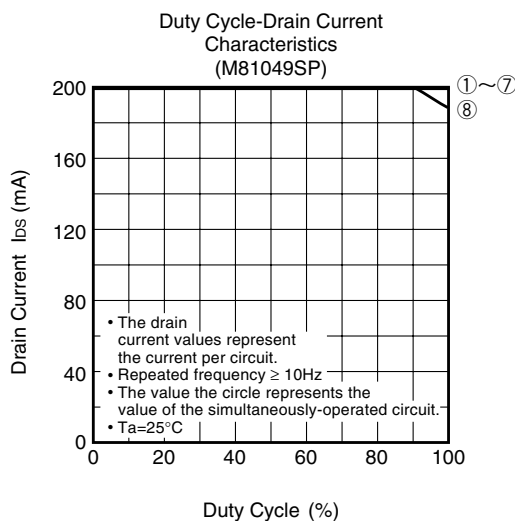
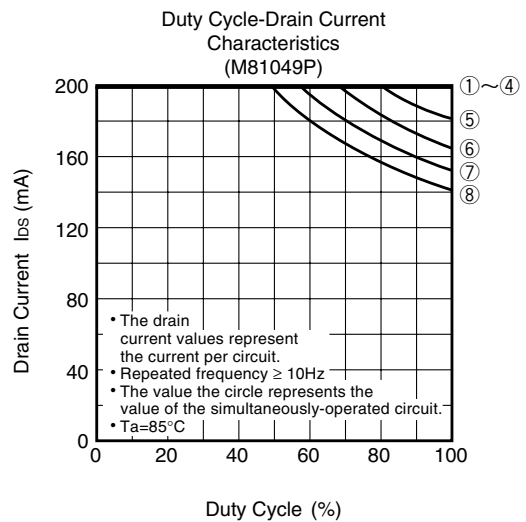
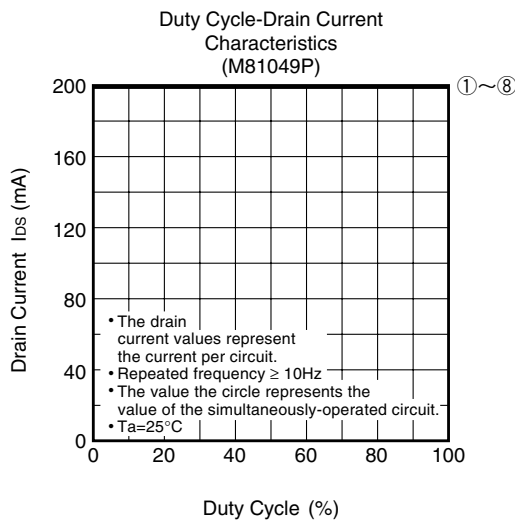
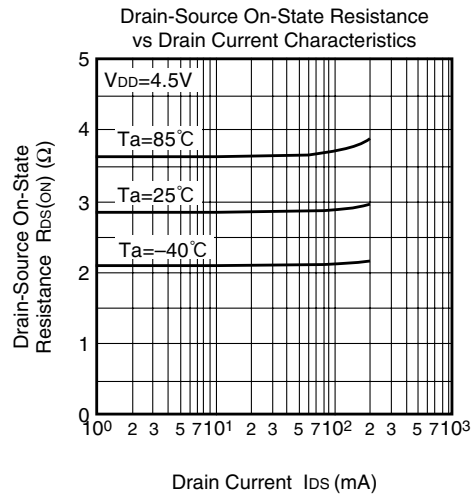
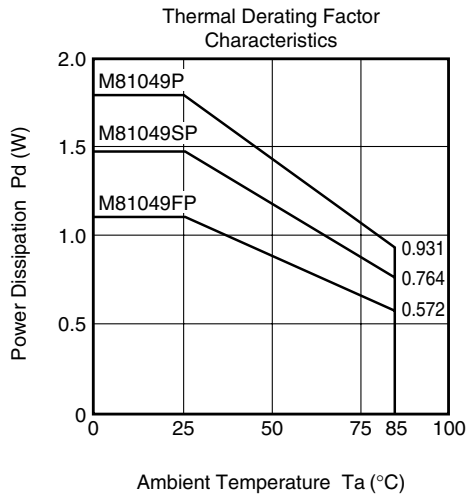


INPUT SETUP AND HOLD WAVEFORMS

**M81049P/SP/FP**

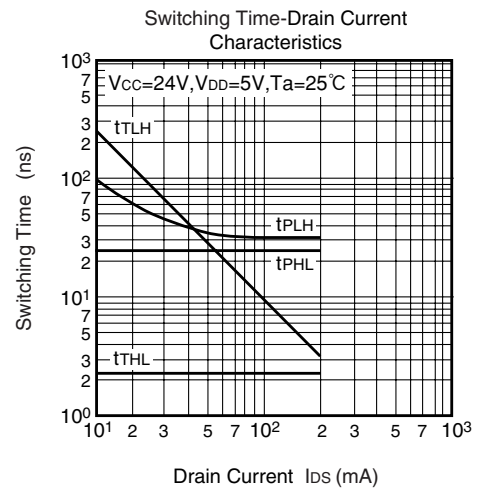
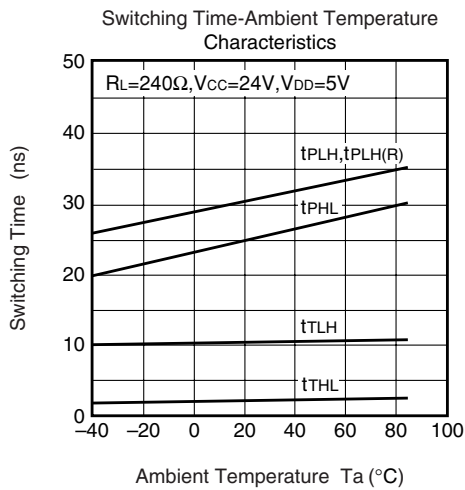
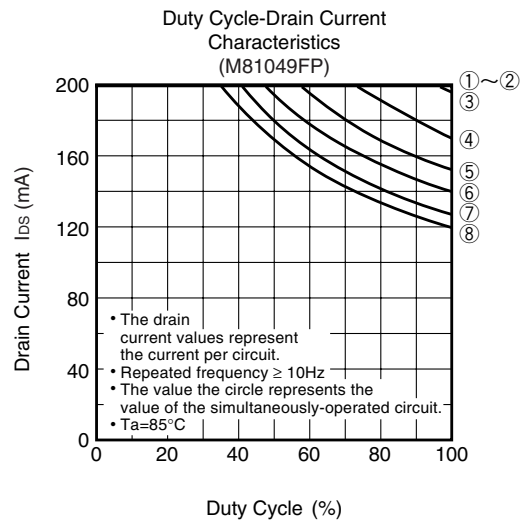
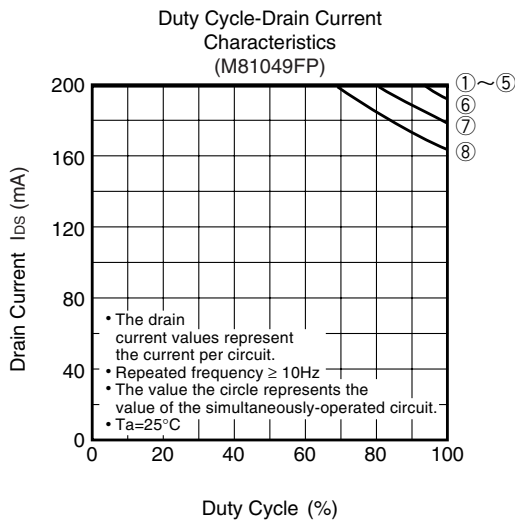
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**TYPICAL CHARACTERISTICS**



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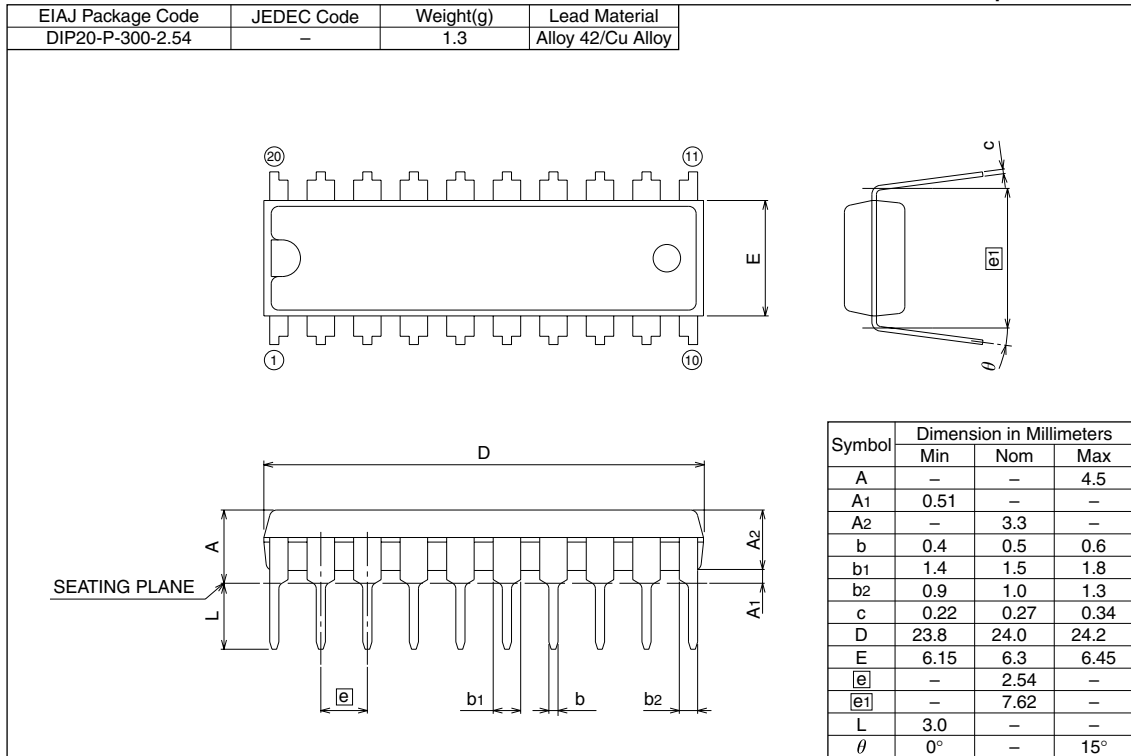


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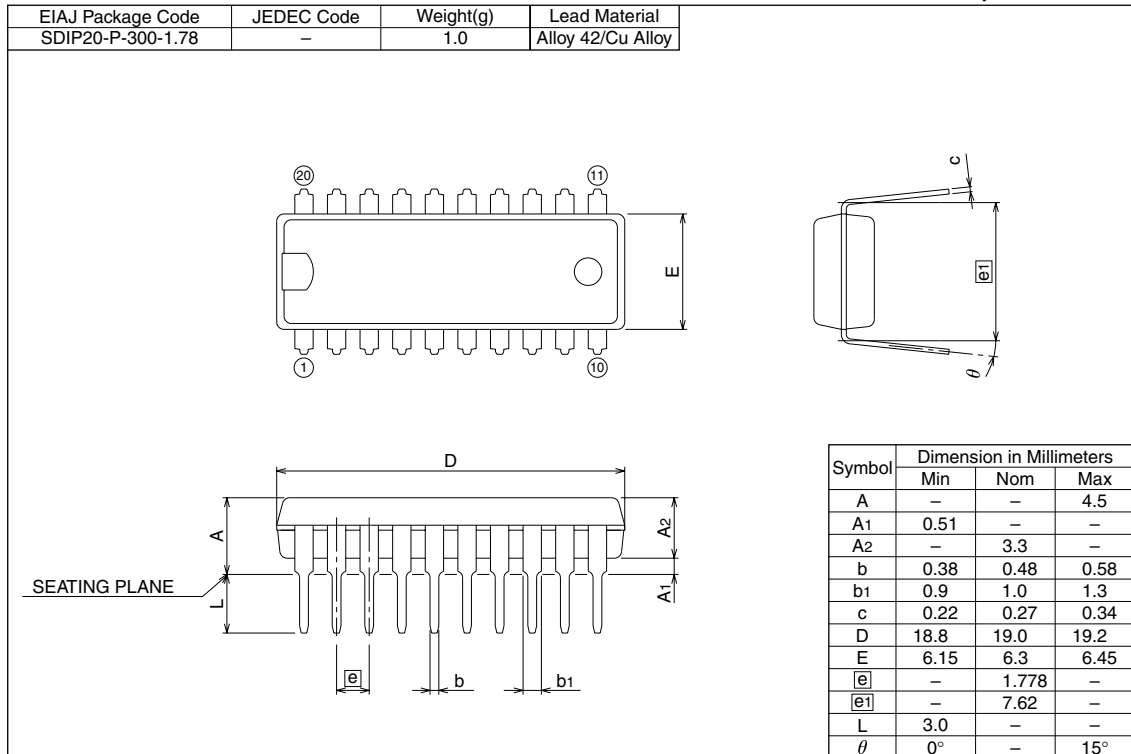
**20P4**

Plastic 20pin 300mil DIP



**20P4B**

Plastic 20pin 300mil SDIP



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OCTAL D-TYPE FLIP-FLOP DRIVER WITH CLEAR

**20P2N-A**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP20-P-300-1.27	-	0.26	Cu Alloy

**Plastic 20pin 300mil SOP**

