From Papilio

Papilio: PapilioPro

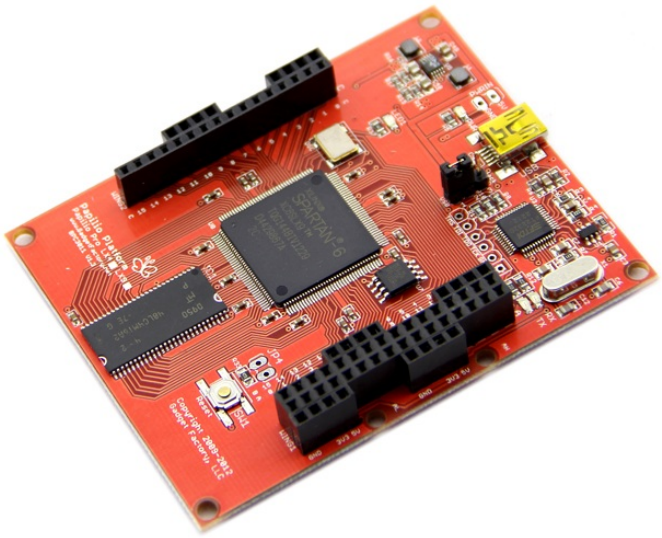
参考資料

Hardware | **Papilio One** - **Papilio Pro** - **MegaWings** - **Wings**

Papilio Pro

The Papilio Pro is an Open Source FPGA development board based on the Xilinx Spartan 6 LX FPGA. It has 48 I/O lines, dual channel USB, integrated JTAG programmer, 64Mb SDRAM, and an efficient switching power supply.

Contents

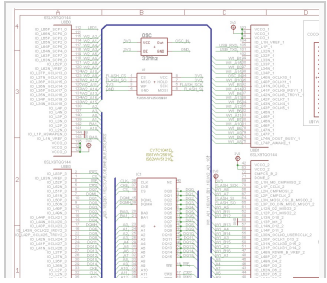


- Spartan 6 LX9 FPGA (**Datasheet**)
- High efficiency LTC3419 Step Down Dual Voltage Regulator (**Datasheet**)
- Dual Channel FTDI FT2232 USB 2.0 Full Speed Interface (**Datasheet**)
- 64Mbit Micron MT48LC4M16 SDRAM (**Datasheet**)
- 64Mbit Macronix MX25L6445 SPI Flash (**Datasheet**)
- 48 I/O pins arranged in a Papilio Wing form factor
- 32Mhz Crystal Oscillator

Spartan 6 LX9 FPGA

The Papilio Pro's **Spartan 6 FPGA** offers some exciting new features over the Spartan 3:

Digital Signal Processing (DSP) Slices
18 DSP48A1 Slices for DSP functions.
Clock Management Tile (CMT)
The Papilio One (Spartan 3E) offered 4 Digital Clock Managers (DCM) but did not offer any Phase-Locked Loops (PLL). The Papilio Pro (Spartan 6) offers the more flexible CMT which provides both DCM's and PLL's!



New I/O Standards
The Papilio Pro (Spartan 6) has direct TMDS I/O support which means that DVI and HDMI interfaces can be implemented without any extra chips.

Multi-Boot Support
You can load multiple bit files into the SPI Flash and setup the first bit file to select which one will be loaded. With some work we could make a ZPUino based bootloader that would have a VGA interface to choose which bit file to load.

BRAM Memory Blocks

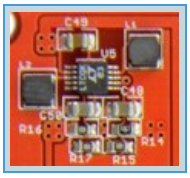
The Spartan 6 allows 18Kbit BRAM blocks to be split into two 9Kbit BRAM blocks.
There is more built in SRAM - there is 64KByte of internal SRAM which is just enough to recreate the Commodore 64!

FPGA Schematic

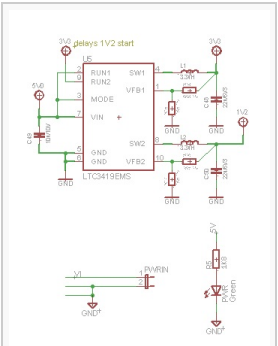
Papilio Board	18Kbit BRAM Blocks	Max SRAM	Usable SRAM
Papilio Pro	32	576Kbit (72KByte)	512Kbit (64KByte)
Papilio One 500K	20	360Kbit (45KByte)	320Kbit (40KByte)
Papilio One 250K	12	216Kbit (27KByte)	192Kbit (24KByte)

BRAM's are 18Kbit in size including two parity bits. In most cases the two parity bits are not used so the BRAM's usable size becomes 16Kbit. If your design can use an 18 bit wide bus then it is possible to utilize the parity bits for data and gain access to all 18Kbit memory space.

Power

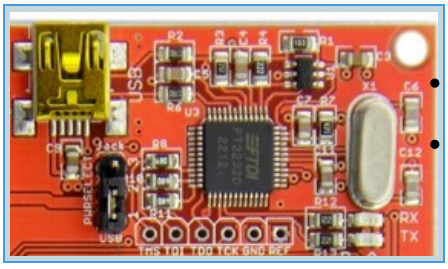


One of the big improvements with the Papilio Pro is its power supply. The Spartan 6 simplifies the power requirements which allowed us to use a high efficiency **LTC3419** switching power supply at about the same component cost as the Papilio One's power supply. The linear regulators used in the Papilio One would noticeably heat up when a complicated, high speed design, like the ZPUino, was running. With the Papilio Pro there is no detectable heat generated, even when the most demanding designs are running!



Power Schematic

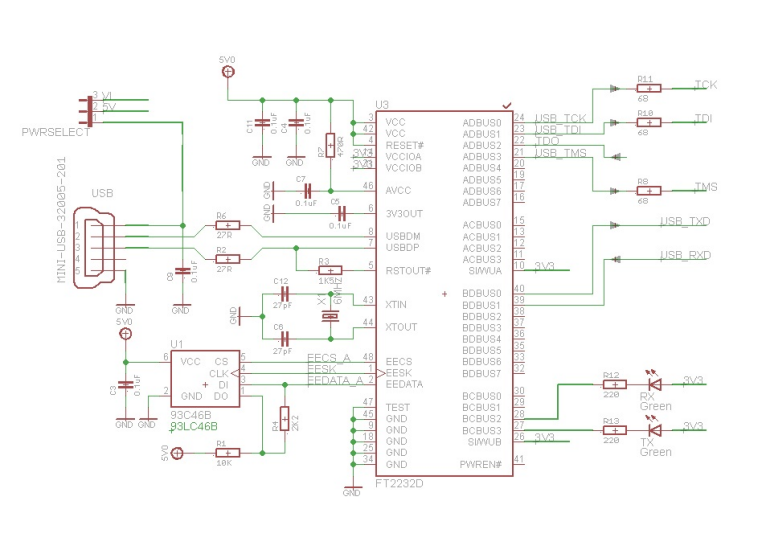
Dual Channel USB



The Papilio Pro uses the same **FT2232** dual channel USB chip that the Papilio One does.

- Channel A is connected to the Papilio Pro in an Asynchronous serial UART configuration that is capable of speeds up to 2MHz.
- Channel B is connected to the JTAG pins of the Papilio Pro and provides very fast programming of the FPGA (500mS).

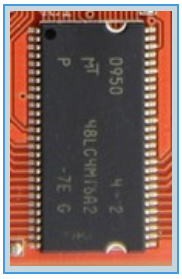
The Papilio Pro includes a reset header (JP4) that can be populated with a jumper to hold the Spartan 6 FPGA in permanent reset mode. This frees up the JTAG Header to be used as an FT2232 JTAG/SPI/MPSSE Programmer.



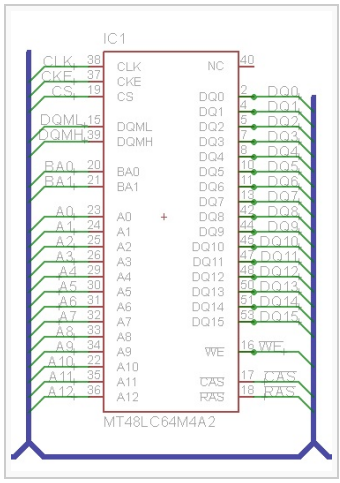
USB Schematic

Name	Direction (FPGA Perspective)	Function	Arduino Pin	Papilio Wing Pin	Papilio Pro Pin
RX	Input	FPGA Serial Receive (MISO)	N/A	N/A	P101
TX	Output	FPGA Serial Transmit (MOSI)	N/A	N/A	P105

SDRAM



The Papilio Pro includes a 64Mbit Micron **MT48LC4M16** SDRAM chip. This additional SDRAM will open up a whole new breed of FPGA applications for the Papilio. The timing requirements and refresh signals of the SDRAM chip do make interfacing it more of a challenge than interfacing regular SRAM, or the internal BRAM. We are working on a SDRAM controller that you can drop into your designs so the SDRAM can be used like regular SRAM.

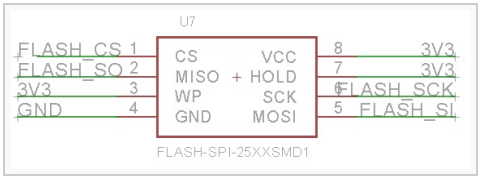


SDRAM Designs

- **Hamster's SDRAM Controller**
- **Alvie's ZPUino SDRAM controller.** (derived from Hamster's SDRAM controller).
- **Wishbone wrapper for Alvie's SDRAM controller.**
- **XAPP 394 Interfacing Mobile SDRAM with CPLD's.**

The ZPUino Soft Processor includes a SDRAM controller which gives your ZPUino sketches 8MByte of code space!

SPI Flash

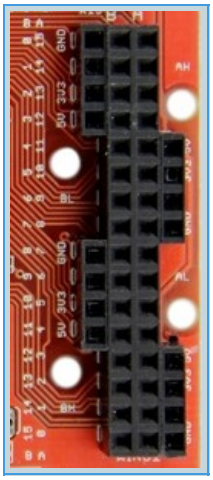


The 64Mbit Macronix **MX25L6445** SPI Flash chip is the largest ever included with a Papilio FPGA. It is the largest available in the 8-SOIC footprint, and is included for good reason! The new multi-boot feature of the Spartan 6 means we can put as many FPGA bit files on the SPI Flash as will fit and use a "golden image" to select which one will boot at startup. Spartan 6 LX9 bit files are 333KBytes in size which means that the Papilio Pro can save up to 23 bit files in SPI Flash. Or, we can save and retrieve user data using techniques like the SmallFS filesystem or **bootstrap code** that loads data from SPI Flash to SRAM at startup.

Name	Direction (FPGA Perspective)	Function	Arduino Pin	Papilio Wing Pin	Papilio Pro Pin
FLASH_CS	Output	SPI Flash Chip Select	N/A	N/A	P38

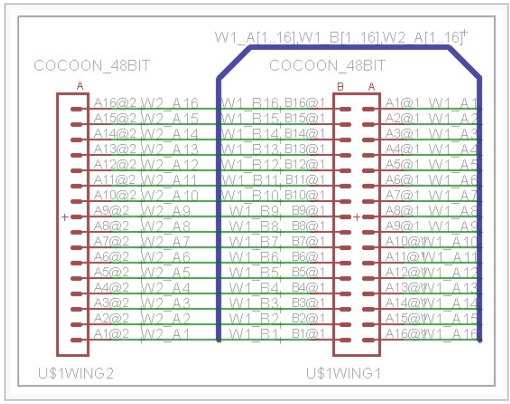
FLASH_CLK	Output	SPI Flash Clock	N/A	N/A	P70
FLASH_MOSI	Output	SPI Flash Master Out Slave In (MOSI)	N/A	N/A	P64
FLASH_MISO	Input	SPI Flash Master In Slave Out (MISO)	N/A	N/A	P65

I/O



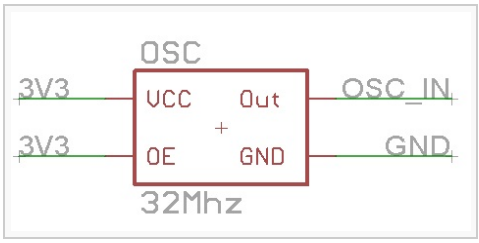
The I/O of the Papilio Pro is backwards compatible with the Papilio One, all existing Papilio Wings and MegaWings work with the Papilio Pro.

The major difference between the Papilio Pro and Papilio One with respect to User I/O is the available voltage levels. The Papilio Pro sets all I/O voltage pins to 3.3V while the Papilio One can switch between 1.2V, 2.5V, and 3.3V. This was a seldom used feature that was dropped in the Papilio Pro for greater compatibility. Additionally, the Papilio Pro does not provide a 2.5V power rail, the 2.5V pin on the Wing Header is left unconnected. There are no Wings or MegaWings that use 2.5V power and there probably never will be... 3.3V seems to be the defacto standard for current peripherals.



Oscillator

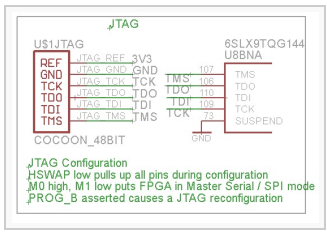
The Papilio Pro has a 32Mhz oscillator that can be converted to any speed desired inside the FPGA using the Clock Management Tile (CMT). There are two PLLs and two **Digital Clock Managers (DCM)** available for your designs.



Name	Direction (FPGA Perspective)	Function	Arduino Pin	Papilio Wing Pin	Papilio Pro Pin
CLK	Input	External 32Mhz Oscillator	N/A	N/A	P94

JTAG

The JTAG header on the Papilio Pro is provided for a couple different reasons:



Use a Xilinx Programming Cable

If you want to use the Xilinx tools such as EDK, Chipscope, or Impact with the Papilio you need a way to use a Xilinx programming cable. The Papilio has a Xilinx JTAG header but the problem is that in the default mode the FT2232D USB chip is connected to the JTAG pins and interferes with programming. What is needed is to put the FT2232 into a mode where the JTAG pins go into High-Z leaving the Xilinx JTAG pins free for the programming cable. To learn more about using a Xilinx Programming Cable visit the **original forum post** or **blog post**.

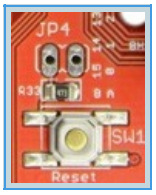
Bypass the FPGA and use the FT2232 as a JTAG/SPI/MPSSE Programmer

The Papilio Pro provides the JP4 pin header, jumping this header will hold the Spartan 6 FPGA in a reset state which frees up the JTAG pins to be controlled by the FT2232. OpenOCD, FlashRAM, and any other FT2232 based software should work directly with this method.

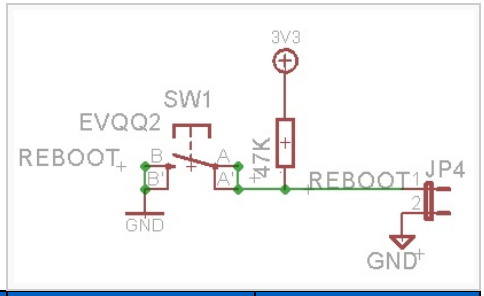
Name	Direction (FPGA Perspective)	Function	Arduino Pin	Papilio Wing Pin	Papilio Pro Pin
JTAG_TMS	Input	JTAG TMS	N/A	N/A	P107
JTAG_TCK	Input	JTAG TCK	N/A	N/A	P109
JTAG_SI	Input	JTAG SI	N/A	N/A	P64

JTAG_SO	Output	JTAG SO	N/A	N/A	P65

Reset



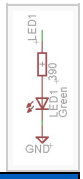
Pressing the reset button will cause the Spartan 6 FPGA to do a hard reset and reload the first bit file from SPI Flash. This is a pretty drastic measure that will wipe out anything running on the FPGA. In most cases it is more desirable to utilize a user button to perform a reset within your design that just initializes all registers to zero.



Name	Direction (FPGA Perspective)	Function	Arduino Pin	Papilio Wing Pin	Papilio Pro Pin
RESET	Input	FPGA Reset	N/A	N/A	P37

User LED

The Papilio Pro provides one user LED that is connected directly to the Spartan 6 FPGA. It is not shared with any of the I/O pins and can be controlled directly from your VHDL or sketches.



Name	Direction (FPGA Perspective)	Function	Arduino Pin	Papilio Wing Pin	Papilio Pro Pin
LED1	Output	USER LED1	N/A	N/A	P112

Links

Papilio Pro Design Files

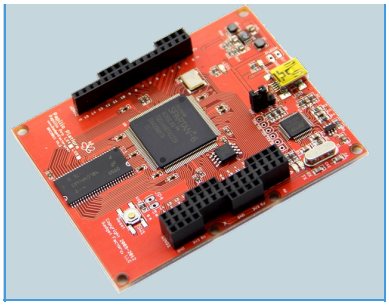
- Papilio Pro Generic User Constraint File (UCF)
- Papilio Pro EAGLE Design Files
- Papilio Pro Schematic (PDF)

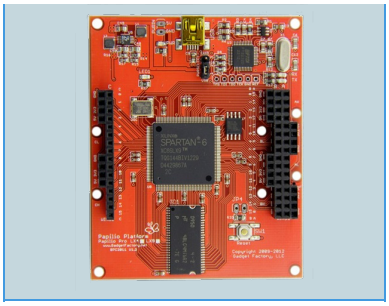
Community Links

- Papilio Pro Project Showcase
- Papilio Pro Forum
- Papilio Pro Downloads

License

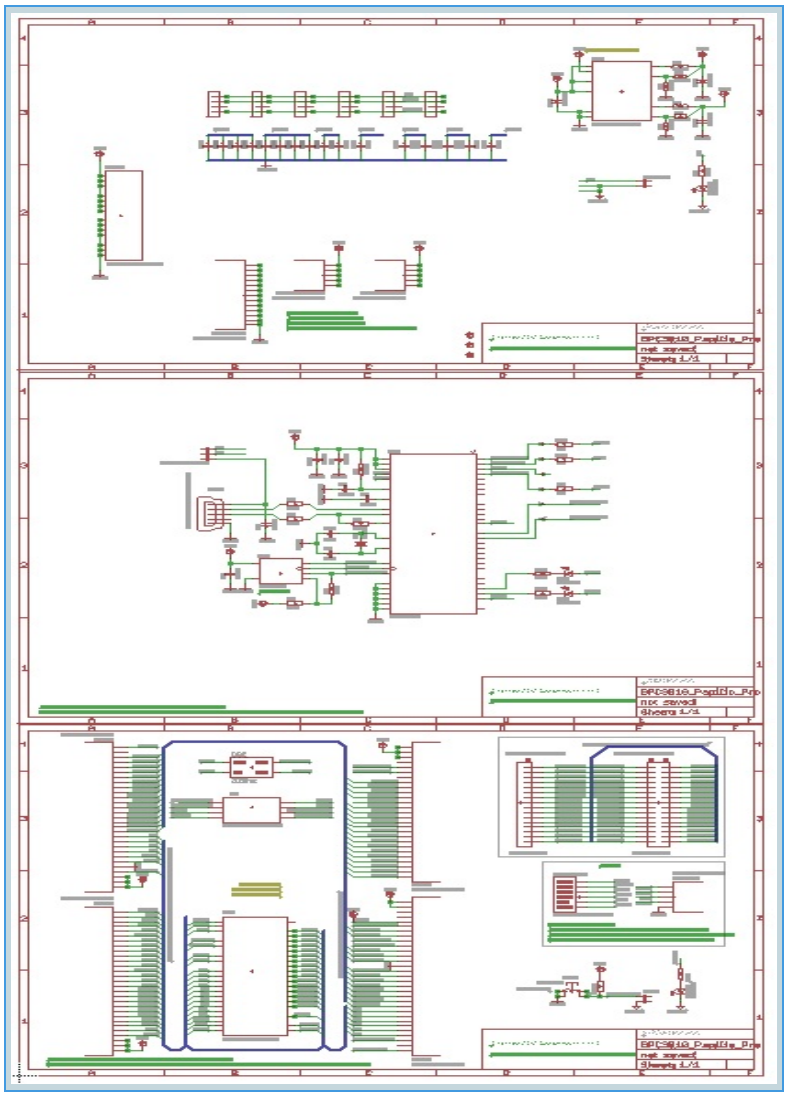
Images





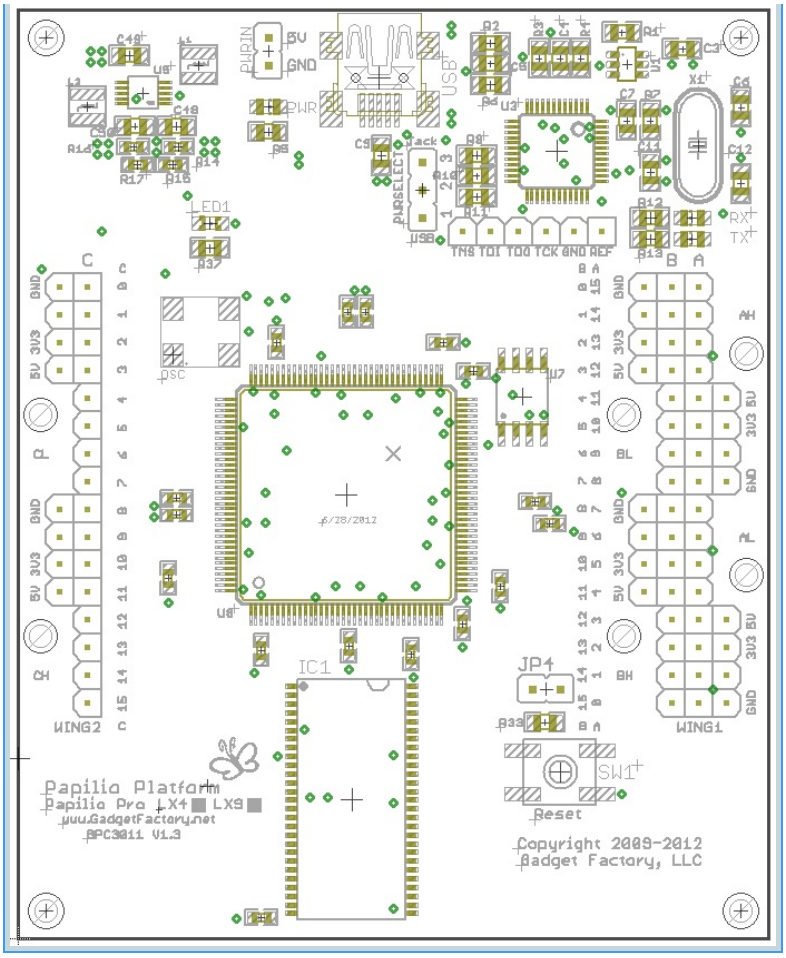
Papilio Pro

Click the images for full size hi-resolution views of the Papilio Pro.



Papilio Pro Schematic

Click the image to load a PDF version of the Papilio Pro Schematic



Assembly View

Click the image for a full size view of the boards part layout.