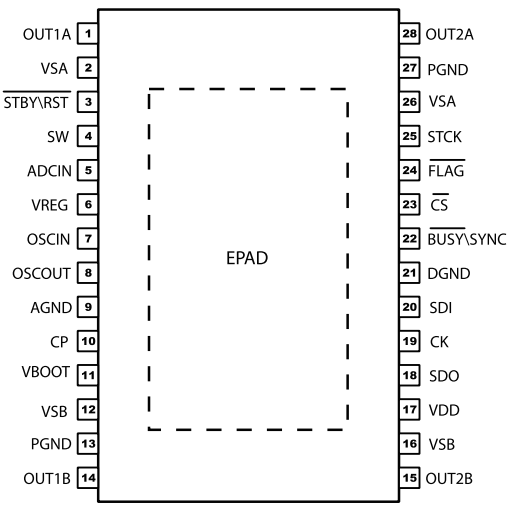
L6470

HTSSOP28

dSPIN™ fully integrated microstepping motor driver with motion engine and SPI

参考資料



Features

- Operating voltage: 8 - 45 V
- 7.0 A out peak current (3.0 A r.m.s.)
- Low $R_{DS(on)}$ Power MOSFETs
- Programmable speed profile and positioning
- Programmable power MOS slew rate
- Up to 1/128 microstepping
- Sensorless stall detection
- SPI interface
- Low quiescent and standby currents
- Programmable non-dissipative overcurrent protection on high and low-side
- Two-levels of overtemperature protection

Applications

- Bipolar stepper motors

Description

The L6470, realized in analog mixed signal technology, is an advanced fully integrated solution suitable for driving two-phase bipolar stepper motors with microstepping. It integrates a dual low $R_{DS(on)}$ DMOS full-bridge with all of the power switches equipped with an accurate on-chip current sensing circuitry suitable for non-dissipative current control and overcurrent protection. Thanks to a unique control system, a true 1/128 steps resolution is achieved. The digital control core can generate user defined motion profiles with acceleration, deceleration, speed or target position, easily programmed through a dedicated registers set. All commands and data registers, including those used to set analogue values (i.e. current control value, current protection trip point, deadtime, PWM frequency, etc.) are sent through a standard 5-Mbit/s SPI. A very rich set of protections (thermal, low bus voltage, overcurrent, motor stall) allows the design of a fully protected application, as required by the most demanding motor control applications.

Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_{DD}	Logic interface supply voltage		5.5	V
V_S	Motor supply voltage	$V_{SA} = V_{SB} = V_S$	48	V
$V_{GND, diff}$	Differential voltage between AGND, PGND and DGND		±0.3	V
V_{boot}	Bootstrap peak voltage		55	V
V_{REG}	Internal voltage regulator output pin and logic supply voltage		3.6	V
V_{ADCIN}	Integrated ADC input voltage range (ADCIN pin)		-0.3 to +3.6	V
V_{OSC}	OSCIN and OSCOUT pin voltage range		-0.3 to +3.6	V
V_{out_diff}	Differential voltage between V_{SA}, $OUT1_A$, $OUT2_A$, PGND and V_{SB}, $OUT1_B$, $OUT2_B$, PGND pins	$V_{SA} = V_{SB} = V_S$	48	V
V_{LOGIC}	Logic inputs voltage range		-0.3 to +5.5	V
I_{out} (1)	R.m.s. output current		3	A
I_{out_peak} (1)	Pulsed output current	T_{PULSE} < 1 ms	7	A
T_{OP}	Operating junction temperature		-40 to 150	°C
T_s	Storage temperature range		-55 to 150	°C
P_{tot}	Total power dissipation (T_A = 25 °C)	(2)	5	W

1. Maximum output current limit is related to metal connection and bonding characteristics. Actual limit must satisfy maximum thermal dissipation constraints.
2. HTSSOP28 mounted on EVAL6470H.

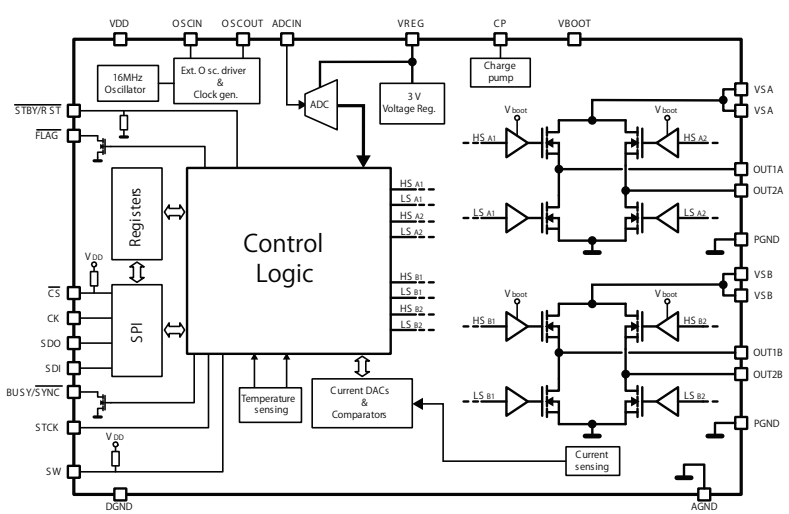
Recommended operating conditions

Symbol	Parameter	Test condition	Value			Unit
V_{DD}	Logic interface supply voltage	3.3 V logic outputs		3.3		V
		5 V logic outputs		5		
V_S	Motor supply voltage	$V_{SA} = V_{SB} = V_S$	8		45	V
V_{out_diff}	Differential voltage between V_{SA}, $OUT1_A$, $OUT2_A$, PGND and V_{SB}, $OUT1_B$, $OUT2_B$, PGND pins	$V_{SA} = V_{SB} = V_S$			45	V
$V_{REG,in}$	Logic supply voltage	V_{REG} voltage imposed by external source	3.2	3.3		V
V_{ADC}	Integrated ADC input voltage (ADCIN pin)		0		V_{REG}	V

Thermal data

Symbol	Parameter	Package	Typ.	Unit
R_{thJA}	Thermal resistance junction-ambient	HTSSOP28 (1)	22	°C/W
		POWERSO36 (2)	12	

1. HTSSOP28 mounted on EVAL6470H rev 1.0 board: four-layer FR4 PCB with a dissipating copper surface of about 40 cm^2 on each layer and 15 via holes below the IC.
2. POWERSO36 mounted on EVAL6470PD rev 1.0 board: four-layer FR4 PCB with a dissipating copper surface of about 40 cm^2 on each layer and 22 via holes below the IC.



ＩＣ底面の放熱パッド（ＥＰＡＤ）とＰＧＮＤ端子（１３，２７）は変換基板上で全て結線されています。ＶＳＡ（２，２６）、ＶＳＢ（１２，１６）、ＶＤＤ（１７）にはそれぞれの端子の間近に０．１μＦの積層セラミックコンデンサが実装されています。

カッコ内は、端子番号または端子名を示します。

また、全ての端子は、２．５４mmピッチにピン配置そのままで引き出されていますので、ユニバーサル基板などで自由に配線することができます。なお、基板には熱伝導性に優れるＥＣＯＯＬ（エクール）Ｒ１７８７を使用しています。

ECOOL
R1787

Pin description

No.		Name	Type	Function
HTSSOP	POWERSO			
17	24	VDD	Power	Logic outputs supply voltage (pull-up reference)
6	9	VREG	Power	Internal 3 V voltage regulator output and 3.3 V external logic supply
7	10	OSCIN	Analog input	Oscillator pin 1. To connect an external oscillator or clock source. If this pin is unused, it should be left floating.
8	11	OSCOUT	Analog output	Oscillator pin 2. To connect an external oscillator. When the internal oscillator is used this pin can supply 2/4/8/16 MHz. If this pin is unused, it should be left floating.
10	13	CP	Output	Charge pump oscillator output
11	14	VBOOT	Supply voltage	Bootstrap voltage needed for driving the high-side power DMOS of both bridges (A and B)
5	8	ADCIN	Analog input	Internal analog-to-digital converter input
2, 26	4, 5, 33, 34	VSA	Power supply	Full-bridge A power supply pin. It must be connected to VSB.
12, 16	15, 16, 22, 23	VSB	Power supply	Full-bridge B power supply pin. It must be connected to VSA.
27, 13	1, 19	PGND	Ground	Power ground pin
1	2, 3	OUT1A	Power output	Full-bridge A output 1
28	35, 36	OUT2A	Power output	Full-bridge A output 2
14	17, 18	OUT1B	Power output	Full-bridge B output 1
15	20, 21	OUT2B	Power output	Full-bridge B output 2
9	12	AGND	Ground	Analog ground.
4	7	SW	Logical input	External switch input pin. If not used the pin should be connected to VDD.
21	28	DGND	Ground	Digital ground
22	29	$\overline{\text{BUSY}}$\SYNC	Open drain output	By default, this BUSY pin is forced low when the device is performing a command. Otherwise the pin can be configured to generate a synchronization signal.
18	25	SDO	Logic output	Data output pin for serial interface
20	27	SDI	Logic input	Data input pin for serial interface
19	26	CK	Logic input	Serial interface clock
23	30	$\overline{\text{CS}}$	Logic input	Chip select input pin for serial interface
24	31	$\overline{\text{FLAG}}$	Open drain output	Status flag pin. An internal open drain transistor can pull the pin to GND when a programmed alarm condition occurs (step loss, OCD, thermal pre-warning or shutdown, UVLO, wrong command, non-performable command)
3	6	$\overline{\text{STBY}}$\$\overline{\text{RST}}$	Logic input	Standby and reset pin. LOW logic level resets the logic and puts the device into Standby mode. If not used, it should be connected to VDD.
25	32	STCK	Logic input	Step-clock input
EPAD	EPAD	Exposed pad	Ground	Internally connected to PGND, AGND and DGND pins

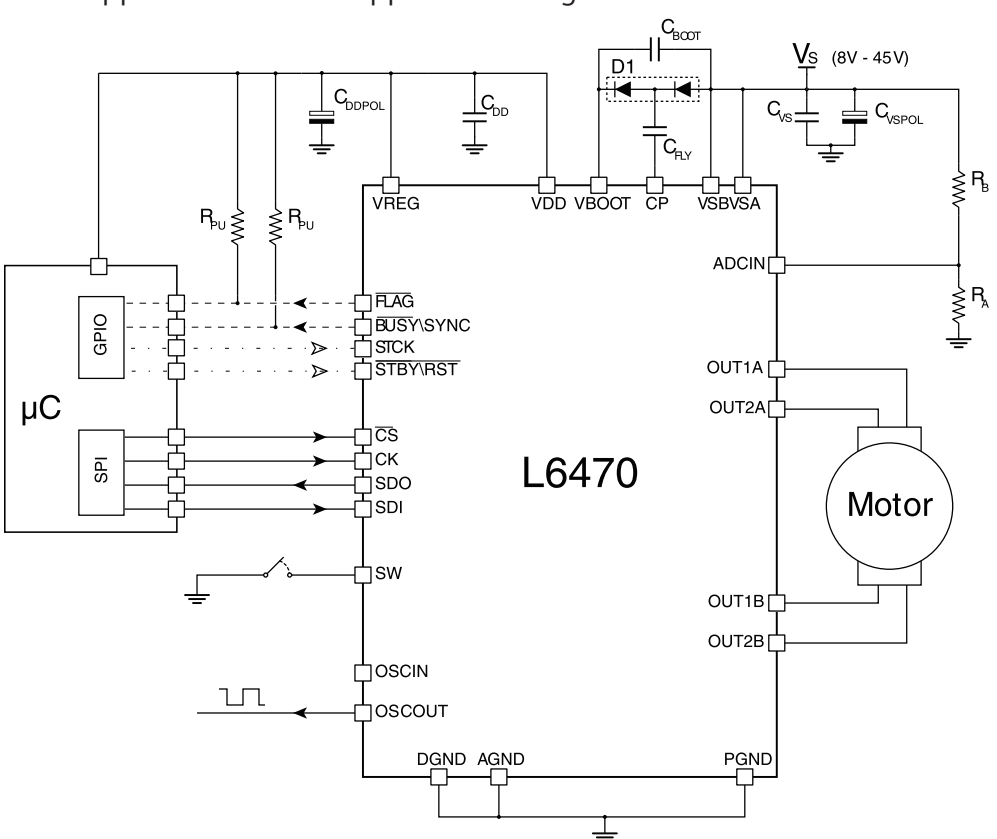
Register map

Address [Hex]	Register name	Register function	Len. [bit]	Reset Hex	Reset value	Remarks (1)
h01	ABS_POS	Current position	22	000000	0	R, WS
h02	EL_POS	Electrical position	9	000	0	R, WS
h03	MARK	Mark position	22	000000	0	R, WR
h04	SPEED	Current speed	20	00000	0 step/tick (0 step/s)	R
h05	ACC	Acceleration	12	08A	125.5e-12 step/tick^2 (2008 step/s^2)	R, WS
h06	DEC	Deceleration	12	08A	125.5e-12 step/tick^2 (2008 step/s^2)	R, WS
h07	MAX_SPEED	Maximum speed	10	041	248e-6 step/tick (991.8 step/s)	R, WR
h08	MIN_SPEED	Minimum speed	13	000	0 step/tick (0 step/s)	R, WS
h15	FS_SPD	Full-step speed	10	027	150.7e-6 step/tick (602.7 step/s)	R, WR
h09	KVAL_HOLD	Holding K_{VAL}	8	29	0.16·VS	R, WR
h0A	KVAL_RUN	Constant speed K_{VAL}	8	29	0.16·VS	R, WR
h0B	KVAL_ACC	Acceleration starting K_{VAL}	8	29	0.16·VS	R, WR
h0C	KVAL_DEC	Deceleration starting K_{VAL}	8	29	0.16·VS	R, WR
h0D	INT_SPEED	Intersect speed	14	0408	15.4e-6 step/tick (61.5 step/s)	R, WH
h0E	ST_SLP	Start slope	8	19	0.038% s/step	R, WH
h0F	FN_SLP_ACC	Acceleration final slope	8	29	0.063% s/step	R, WH
h10	FN_SLP_DEC	Deceleration final slope	8	29	0.063% s/step	R, WH
h11	K_THERM	Thermal compensation factor	4	0	1.0	R, WR
h12	ADC_OUT	ADC output	5	XX (2)		R
h13	OCD_TH	OCD threshold	4	8	3.38A	R, WR
h14	STALL_TH	STALL threshold	7	40	2.03A	R, WR
h16	STEP_MODE	Step mode	8	7	128 microsteps	R, WH
h17	ALARM_EN	Alarm enable	8	FF	All alarms enabled	R, WS
h18	CONFIG	IC configuration	16	2E88	Internal oscillator, 2 MHz OSCOUT clock, supply voltage compensation disabled, overcurrent shutdown enabled, slew rate = 290 V/µs PWM frequency = 15.6 kHz.	R, WH
h19	STATUS	Status	16	XXXX (2)	High impedance state, UVLO/Reset flag set.	R
h1A	RESERVED	Reserved address				
h1B	RESERVED	Reserved address				

1. R: readable, WH: writable only when outputs are in high impedance, WS: writable only when motor is stopped, WR: always writable.
2. According to startup conditions.

Bipolar stepper motor control application using L6470

参考資料



Typical application values

Name	Value
C_{VS}	220 nF
C_{VSPOL}	100 µF
C_{REG}	100 nF
C_{REGPOL}	47 µF
C_{DD}	100 nF
C_{DDPOL}	10 µF
D1	Charge pump diodes
C_{BOOT}	220 nF
C_{FLY}	10 nF
R_{PU}	39 kΩ
R_{SW}	100 Ω
C_{SW}	10 nF
R_A	2.7 kΩ (VS = 36 V)
R_B	62 kΩ (VS = 36 V)