

**General Description**

The AL1402 OptoRec interface decodes four stereo pairs (8 channels) of digital audio from a single ADAT® Optical data stream formatted as described in U.S. patent number 5,297,181.

A companion encoder, the AL1401A OptoGen™ is also available.

Use of the ADAT Optical interface (including the OptoGen and OptoRec) requires a license agreement (generally royalty-free) between the manufacturer and Wavefront Semiconductor. Details and agreement information are available upon request from Wavefront directly, or on our web site.

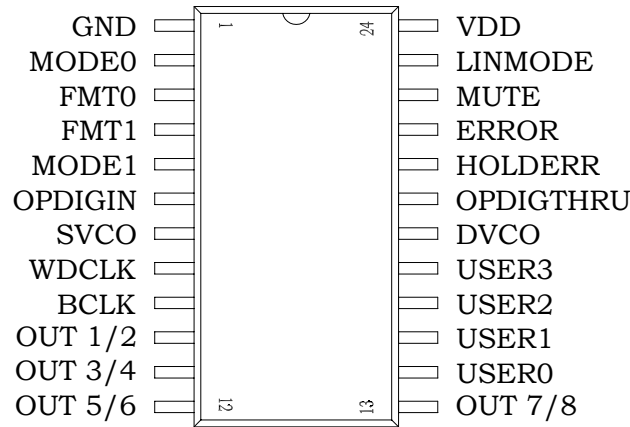
**Features**

- ❑ Compatible with ADAT® Type I and II formats
- ❑ 4 stereo pairs as outputs using standard ADC formats
- ❑ 4 user bit outputs to receive time-code, MIDI data, etc.
- ❑ Internal PLL generates required clocks from optical data.
- ❑ Word Clock input to synchronize outputs to user's system.

**Applications**

- ❑ Digital Mixing Boards
- ❑ Signal Processors
- ❑ Digital Effects Boxes
- ❑ Digital Recorders
- ❑ Computer Sound Boards
- ❑ Sound Reinforcement Products

**Package and pinout**



24 pin  
SOIC

## Pin Descriptions

Pin #	Name	Pin Type	Description
1	GND	Power	Ground pin
2	MODE0	Input	Mode select
3	FMT0	Input	Format select
4	FMT1	Input	Format select
5	MODE1	Input	Mode select
6	OPDIGIN	Input	Input from optical receiver
7	SVCO	Output	Derived clock from WDCLK in slave mode; derived from DVCO in Master mode (nominal 12.288MHz, 256x Fs)
8	WDCLK	I/O	Input or output word clock, see Table 4, Modes (nominal 48KHz, Fs)
9	BCLK	Output	Bit clock (nominal 3.072MHz, 64 x Fs)
10	OUT 1/2	Output	Channels 1 and 2 data output
11	OUT 3/4	Output	Channels 3 and 4 data output
12	OUT 5/6	Output	Channels 5 and 6 data output
13	OUT 7/8	Output	Channels 7 and 8 data output
14	USER0	Output	USER0 data bit output. Used to receive timecode
15	USER1	Output	USER1 data bit output. Used to receive MIDI data.
16	USER2	Output	USER2 data bit output. Reserved.
17	USER3	Output	USER3 data bit output. Reserved.
18	DVCO	Output	Recovered clock from data stream(nominal 12.288MHz, 256 x Fs)
19	OPDIGTHRU	Output	OPDIGIN is regenerated and clocked out on this pin to allow daisy-chaining
20	HOLDERR	Input	If high, the ERROR pin stays high until the cause of the error is removed AND the HOLDERR pin goes low.
21	ERROR	Output	Indicates lack of input or failure to synchronize to data stream, mutes data outputs but not clock outputs
22	MUTE	Input	If high, mutes outputs
23	LINMODE	Input	Tie high
24	V <sub>DD</sub>	Power	+5V power pin

## Electrical Characteristics and Operating Conditions

Symbol	Description	Min	Typ	Max	Units
<b>Recommended Operating Conditions</b>					
V <sub>DD</sub>	Supply Voltage	4.5	5.0	5.5	V
I <sub>DD</sub> Master	Supply Current, Master	-	7.7	-	mA
I <sub>DD</sub> Slave	Supply Current, Slave	-	5.4	-	mA
F <sub>s</sub>	Sample rate	30	48	55	kHz
Temp	Temperature	0	25	70	°C

Symbol	Description	Min	Typ	Max	Units
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**Inputs (WDCLK, FMT, OPDIGIN, MODE, LINMODE, MUTE, HOLDERR)**

V <sub>IH</sub>	Logical “1” input voltage	0.75 V <sub>DD</sub>	-	-	V <sub>DD</sub>
V <sub>IL</sub>	Logical “0” input voltage	-	-	0.25 V <sub>DD</sub>	V <sub>DD</sub>
I <sub>IH</sub>	Logical “1” input current	-	-	1	uA
I <sub>IL</sub>	Logical “0” input current	-	-	1	uA
C <sub>IN</sub>	Logic Input Capacitance	-	5	-	pF

**Outputs (WDCLK, DVCO, OPDIGTHRU, SVCO, BCLK, ERROR)**

V <sub>OH</sub>	Logical “1” output voltage	0.9 V <sub>DD</sub>	-	-	V <sub>DD</sub>
V <sub>OL</sub>	Logical “0” output voltage	-	-	0.1 V <sub>DD</sub>	V <sub>DD</sub>
I <sub>OH</sub>	Logical “1” output current	-	-	-8	mA
I <sub>OL</sub>	Logical “0” output current	-	-	8	mA

**Outputs (OUT, USER)**

V <sub>OH</sub>	Logical “1” output voltage	0.9 V <sub>DD</sub>	-	-	V <sub>DD</sub>
V <sub>OL</sub>	Logical “0” output voltage	-	-	0.1 V <sub>DD</sub>	V <sub>DD</sub>
I <sub>OH</sub>	Logical “1” output current	-	-	-2	mA
I <sub>OL</sub>	Logical “0” output current	-	-	2	mA

## Master and Slave Modes

### Master Mode:

All outputs are derived from the input optical format data stream on the OPDIGIN (pin 6). WDCLK is an output.

### Slave Mode:

DAC outputs, USER outputs, BCLK and SVCO outputs are synchronized to WDCLK, which is an input.

In Slave mode, WDCLK may be at an arbitrary phase with respect to the incoming samples of OPDIGIN, but if the frequencies aren't identical samples will be dropped, repeated, or garbled. Generally, identical frequencies are achieved by either: using DVCO (pin 18) as the source from which WDCLK is generated, or creating OPDIGIN from a source synchronized to WDCLK.

## Applications Information

The AL1402 OptoRec interface has been designed for ease of use and flexibility in systems designed to interface to the ADAT® protocol. It supports both left and right justified data formats for ease of integration into existing devices as well as new devices. These formats allow it to operate in parallel with many standard ADC's.

The designer uses the FMT0, FMT1, MODE0 and MODE1 pins to select the desired format and mode.

The format pins are summarized in Table 3, Formats. The AL1402 provides support for both the ADAT® Type I format (16-bit) and the ADAT® Type II format (20-bit). Data output is 24 bit. Data input lengths up to 24 bits is supported.

USER0 is used to receive the ADAT® format 32-bit timcode; USER1 is used to receive MIDI data (if the source device supports these features). USER2 and USER3 are reserved and should not be used.

**Formats**

FMT1	FMT0	Format
0	0	OUT data is right justified, BCLK falls on changing WDCLK
0	1	OUT data is left justified, BCLK rises on changing WDCLK
1	0	Chip Reset
1	1	Gated BLCK, BCLK rises on changing WDCLK

**Modes**

MODE1	MODE0	Mode
0	0	Master mode, WDCLK is an output
0	1	Slave mode, WDCLK is an input. WDCLK MUST be derived from the same clock supplying the source
1	0	Reserved
1	1	Reserved

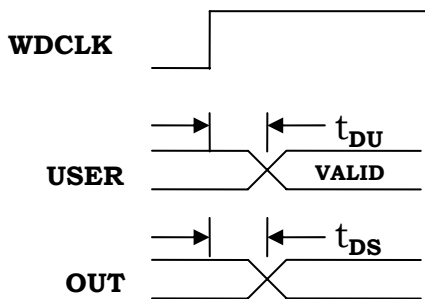
**TIMING**

**Output Delay**

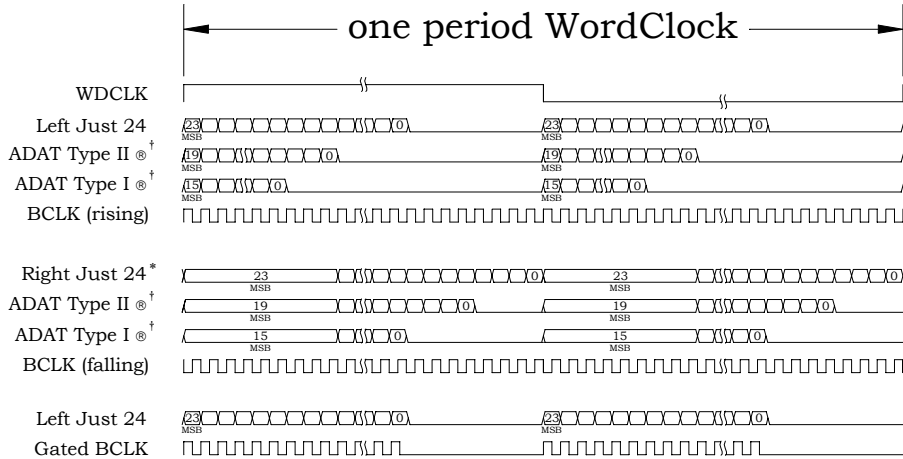
Symbol	Min	Typ	Max	Units
$t_{DU}(\text{Master})$	-10	2	27	nsec
$t_{DU}(\text{Slave})$	-7	5	30	nsec
$t_{DS}(\text{Master})$	-10	0	25	nsec
$t_{DS}(\text{Slave})$	-8	2	27	nsec

Note: Above specifications hold after 3900 WDCLK cycles of valid input at OPDIGIN

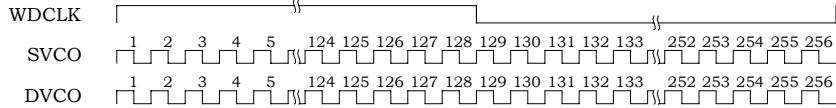
**LEFT CHANNEL (example)**



## Output Timing Diagrams



### Master Mode

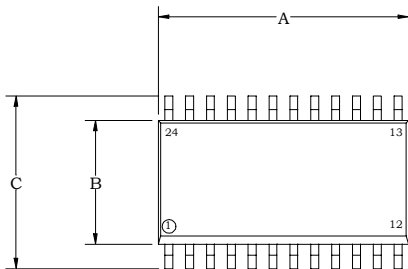


### Slave Mode

In Slave mode DVCO is not phase aligned with WDCLK and SVCO.

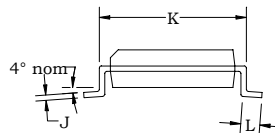
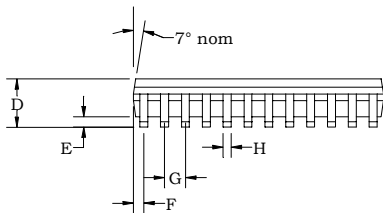
- \* MSB bit is sign extended to left of frame.
- † These diagrams represent how data would be framed from an ADAT type I or type II device. They are not actual modes of the AL1402. The Left Justified Mode is recommended for ADAT formats.

## Package Information

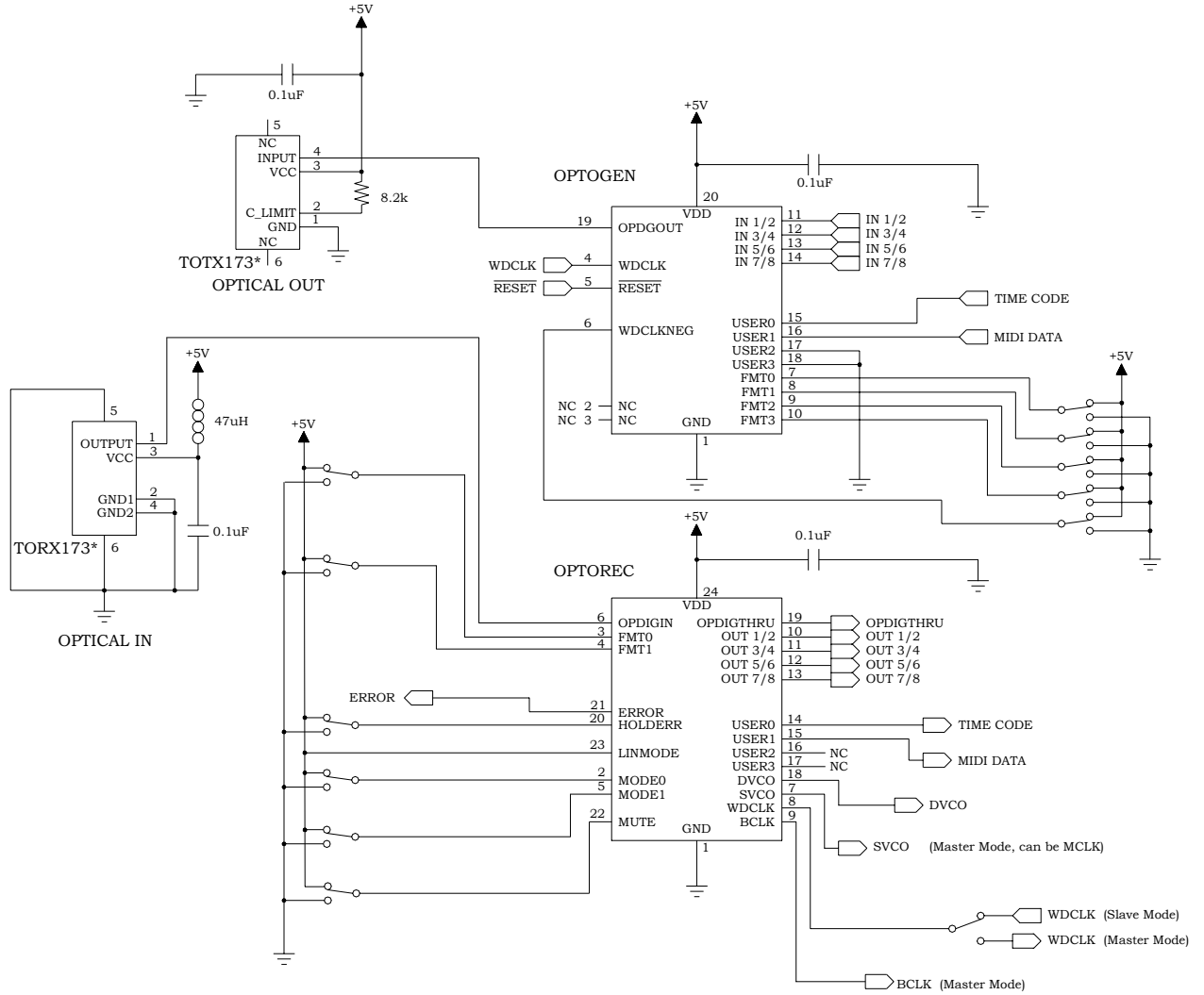


	Dimensions (Typical)	
	Inches	Millimeters
A	.606"	15.40
B	.295"	7.50
C	.406"	10.30
D	.100"	2.50
E	.008"	0.20
F	.025"	0.64
G	.050"	1.27
H	.017"	0.42
J	.011"	0.27
K	.352"	8.94
L	.033"	0.83

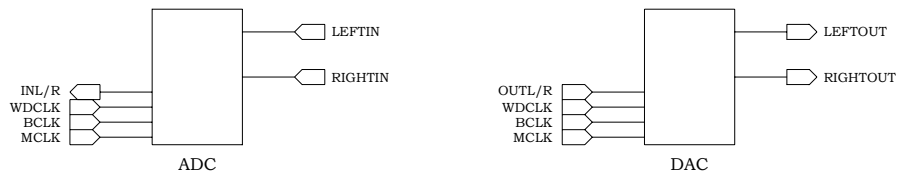
Note: Dimension "A" does not include mold flash, protrusions or gate burrs.



## Sample Application Schematic



\* Optical I/O parts shown are Toshiba parts. The Sharp GP1F33RT or equivalent is also compatible.



The OptoGen accepts input from an ADC, then outputs the Alesis optical format. The OptoRec accepts input in Alesis optical format, then outputs to a DAC.

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