coolaudio

ADAT Optical Audio Data Generator and Encoder

V1401

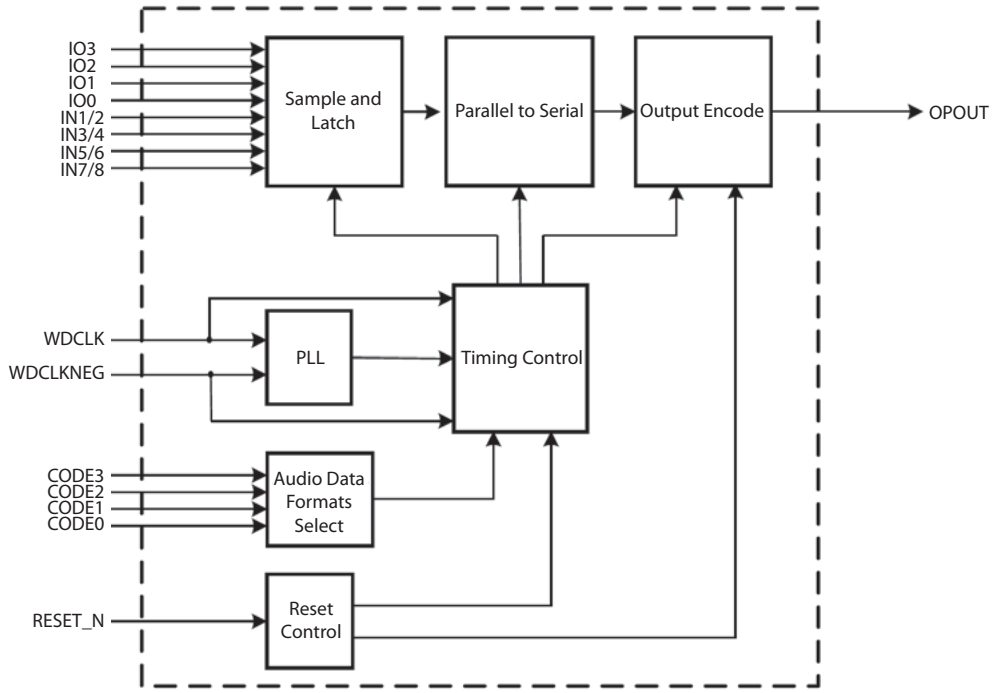
1. Overview

The V1401 encodes four stereo pairs of digital audio (8 channels, both left and right justified 16, 18, 20, 22 and 24-bit data formats are supported) and four IO data bits, producing a single data stream suitable for transmission according to the industry-standard ADAT Optical protocol. It is applied in digital mixing boards, signal processors and sound reinforcement products, etc. V1401 features are:

- Compatible with ADAT Type I (16-bit) and II (20-bit) formats
- 4 stereo pairs as inputs using standard DAC formats
- Both left and right justified 16, 18, 20, 22 and 24-bit data formats are supported
- 4 IO data inputs to transmit time-code, MIDI data, etc.
- Internal PLL generates all required clocks with a word clock input
- Package: SOP20

2. Block Diagram and Pin Description

2.1 Block DiagramF



2.2 Block Description

The V1401 Optical Audio Data Generator interface encodes four stereo pairs of digital audio (8 channels) and four IO data bits, produces a single data stream in the ADAT Optical format. This data stream can be transmitted on the optical transmitters to the corresponding optical receiver interface.

The internal PLL locks to the rising edge of WDCLK and realizes 256 multiple of frequency. Then the sample clocks of input data and control signals needed are derived from the output of PLL by the timing control circuitry. These necessary high frequency clocks and timing signals are used to control the sample and latch circuitry and parallel to serial circuitry. Four stereo pairs of digital audio (8 channels) and four IO data bits are encoded to a serial data stream with all data information through these circuits. No Return Zero Inverse (NRZI) encoding of this data stream is realized through output encode circuitry. Finally, the device outputs a data stream in the ADAT Optical format which is suitable for far distance optical transmission.

The specific input format of the digital audio data to be used is selected by the format pins CODE3 to CODE0, both left and right justified 16, 18, 20, 22 and 24-bit data formats are supported. The internal timing control circuitry will provide corresponding sample clocks and control signals to sample and latch circuitry, thus encoding of digital audio with different data formats is realized.

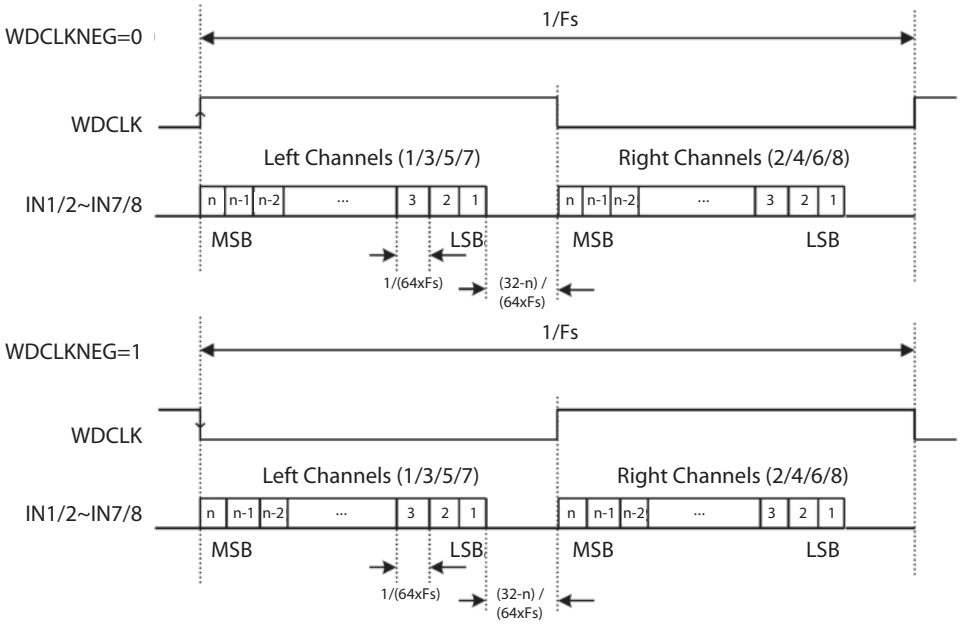
2.2.1 Input data formats selection

Both left and right justified 16, 18, 20, 22 and 24-bit data formats are supported in V1401. These formats allow it to match with different devices, and get a flexible application in systems compatible with ADAT protocol. Besides, the device can operate in parallel with many standard DACs.

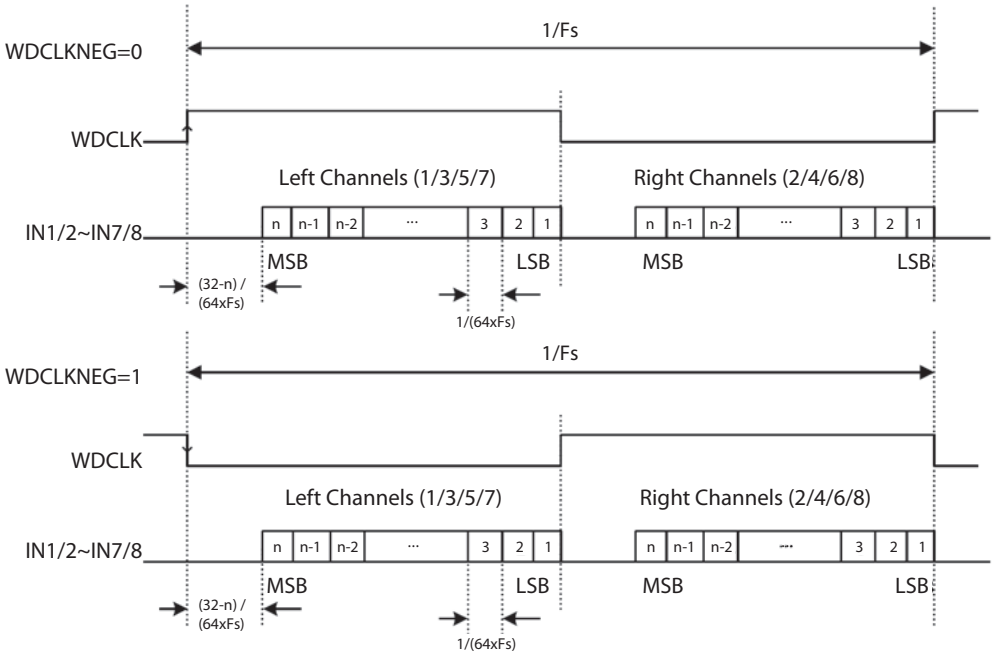
The specific input format (for IN1/2~IN7/8) to be used is selected by the format pins CODE3 to CODE0. These data input formats are outlined in following table.

CODE [3:0]	Input Formats (for IN1/2~IN7/8)
0000	16-bit right justified
0001	18-bit right justified
0010	20-bit right justified
0011	22-bit right justified
0100	16-bit left justified
0101	18-bit left justified
0110	20-bit left justified
0111	22-bit left justified
1000	Reserved
1001	Reserved
1010	Reserved
1011	Reserved
1100	24-bit right justified
1101	24-bit left justified
1110	Reserved
1111	Mute: the digital audio data is screened

With the use of the WDCLKNEG input, the user may choose the phase of the word clock to apply to the device. When WDCLKNEG is low, V1401 will expect the rising edge of WDCLK to signal a new period. When WDCLKNEG is high, V1401 will expect the falling edge of WDCLK to signal a new period. In both cases, the first sample data received is the odd numbered (left) channel, and the second is the even numbered (right) channel. Different input formats are shown in following figures.



(1) n-bit left justified (n=16, 18, 20, 22, 24)

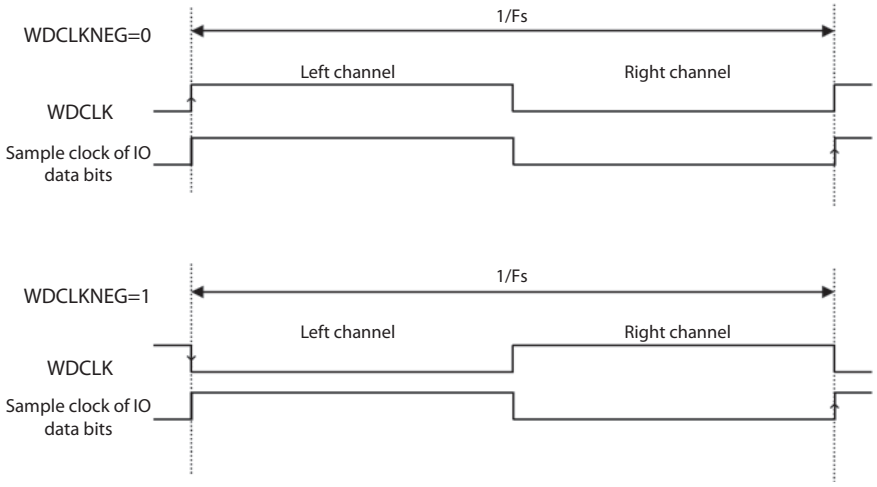


(2) n-bit right justified (n=16, 18, 20, 22, 24)

The device will provide sample clocks corresponding to the selected input format to sample and latch these four stereo pairs of digital audio data correctly. The sampling frequency is 64×Fs (3.072 MHz) with input frequency as Fs (48 kHz).

2.2.2 ADAT Optical Data Stream

In the four IO data inputs, IO0 is used to transmit the ADAT format 32-bit timecode, IO1 is used to transmit MIDI data, IO2 indicates the presence of S/Mux data, IO3 is reserved and should be tied low. The sampling frequency of these IO data inputs is Fs (48 kHz). All IO data bits are sampled at the WDCLK edge that indicates the end of right channel data. It is shown in following figures.



V1401 samples and encodes four stereo pairs of digital audio (8 channels) and four IO data bits, produces a single data stream in ADAT Optical format.

2.2.3 Reset circuitry

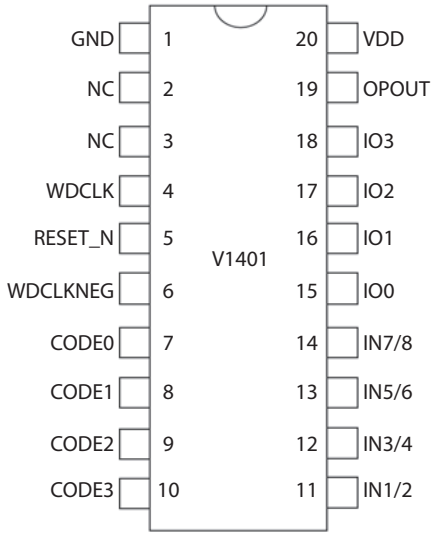
The Reset pin (RESET_N) of V1401 is asynchronous, and a minimum pulse width of 10ns is sufficient. If the reset is active (low), the device will be in a reset state in which all state registers are in their initial state and the OPOUT data stream is invalid. However, PLL lock will not be disturbed.

2.2.4 Internal PLL

The device contains an internal PLL that locks to the rising edge of WDCLK, realizes 256 multiple of frequency, and produces all necessary high frequency clocks and timing signals to operate the device. This high quality PLL will reject any high-frequency jitter on the incoming wordclock. Receiving a crystal-derived 48 kHz on WDCLK, and audio data on all 8 input channels, the jitter was measured to be 630 ps typical on OPOUT.

The PLL allows a simplified user interface and eliminates the need of running high frequency clocks to the part on PCB traces. This reduces unwanted RF noise and coupling problems that can occur when such clock signals are required on input pins for a device.

2.3 Pin Configuration



2.4 Pin Description

Pin	Symbol	Function	Attribute
1	GND	Ground connection	S
2, 3	NC	No connect	
4	WDCLK	Word clock input (normal 48kHz, Fs)	I
5	RESET_N	Reset input, active low	I
6	WDCLKNEG	Word clock phase select: 0: Rising edge of WDCLK to start a new period 1: Falling edge of WDCLK to start a new period	I
7	CODE0	Sets data format of four stereo pairs of digital audio	I
8	CODE1	Sets data format of four stereo pairs of digital audio	I
9	CODE2	Sets data format of four stereo pairs of digital audio	I
10	CODE3	Sets data format of four stereo pairs of digital audio	I
11	IN1/2	Channels 1 and 2 data input	I
12	IN3/4	Channels 3 and 4 data input	I
13	IN5/6	Channels 5 and 6 data input	I
14	IN7/8	Channels 7 and 8 data input	I
15	IO0	IO0 data bit input. Used to transmit timecode	I
16	IO1	IO1 data bit input. Used to transmit MIDI data	I
17	IO2	IO2 data bit input. Used to indicate S/Mux	I
18	IO3	IO3 data bit input. Reserved, tie low	I
19	OPOUT	Output to optical transmitter	O
20	VDD	The positive supply	S

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Unless otherwise specified, T_{amb} = 25 °C

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 ~ 5.5	V
Input/Output Voltage	V_{IN} / V_{OUT}	GND – 0.3 ~ VDD + 0.3	mA
Operating Temperature	T_{amb}	0 ~ 70	°C
Storage Temperature	T_{stg}	-65 ~ 150	°C

3.2 Electrical Characteristics

3.2.1 DC Parameter

Unless otherwise specified, T_{amb} = 25 °C

Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current	I_{DD}	V_{DD} = 5 V		1.5		mA
Ground	GND		—	0.0	—	V
Sample rate	Fs	V_{DD} = 5 V	30	48	55	kHz
Temperature	Temp		0	25	70	°C
Inputs (WDCLK, WDCLKNEG, CODE0~CODE3, IN1/2~IN7/8, IO0~IO3, RESET_N)						
Logical “1” input voltage	V_{IH}	V_{DD} = 5 V	0.75 V_{DD}			V
Logical “0” input voltage	V_{IL}	V_{DD} = 5 V			0.25 V_{DD}	V
Logical “1” input current	I_{IH}	V_{DD} = 5 V			1	µA
Logical “0” input current	I_{IL}	V_{DD} = 5 V			1	µA
Logical input capacitance	C_{IN}			5		pF
Output (OPOUT)						
Logical “1” output voltage	V_{OH}	V_{DD} = 5 V	0.9 V_{DD}			V
Logical “0” output voltage	V_{OL}	V_{DD} = 5 V			0.1 V_{DD}	V
Logical “1” output current	I_{OH}	V_{DD} = 5 V V_{OH} = 4.5 V			-8	mA
Logical “0” output current	I_{OL}	V_{DD} = 5 V V_{OH} = 0.5 V			8	mA

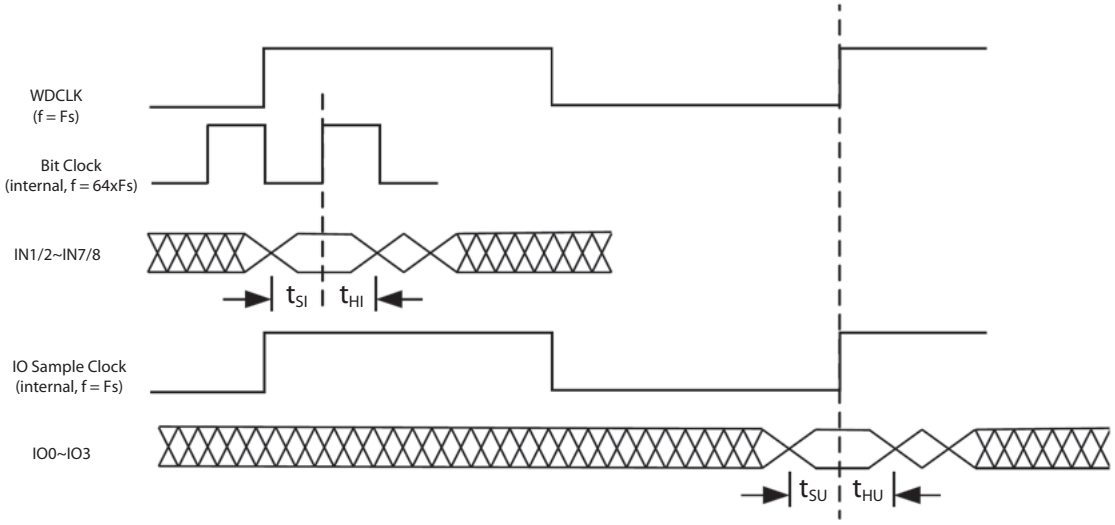
3.2.2 AC Parameter

Unless otherwise specified, Tamb = 25 °C

Parameter	Sym.	Min.	Typ.	Max.	Unit
IN1/2~IN7/8 setup time relative to bit sample clock	t_{SI}		10	30	ns
IN1/2~IN7/8 hold time relative to bit sample clock	t_{HI}		10	30	ns
IO0~IO3 setup time relative to IO sample clock	t_{SU}			100	ns
IO0~IO3 hold time relative to IO sample clock	t_{HU}			100	ns

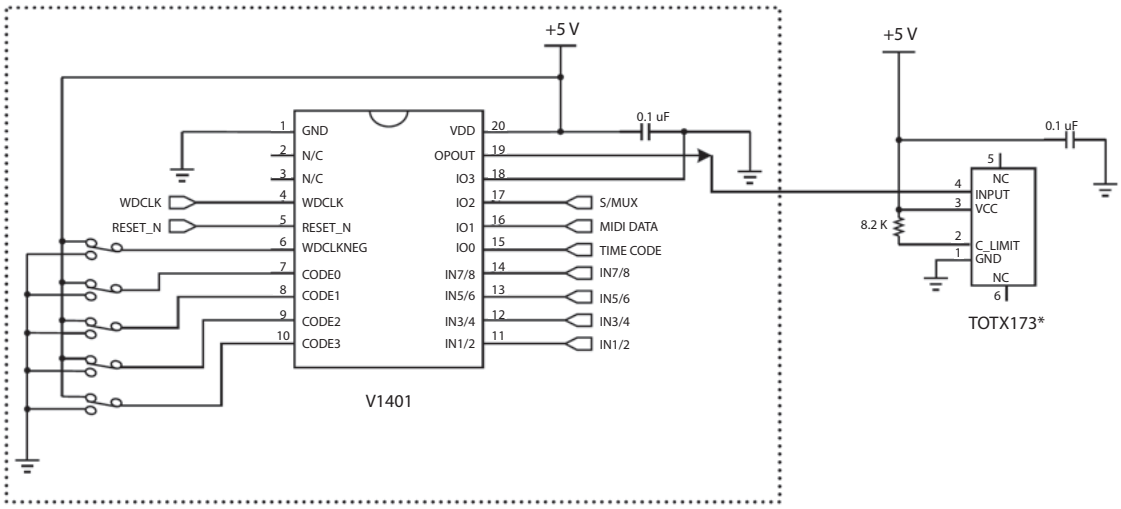
Note: Above specifications hold after 2000 WDCLK cycles

A Timing Diagram for Data Sampling



4. Typical Application Circuit and Information

4.1 Application Circuit

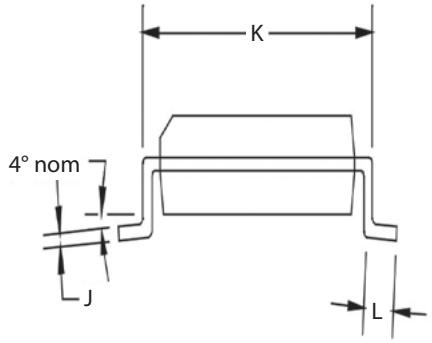


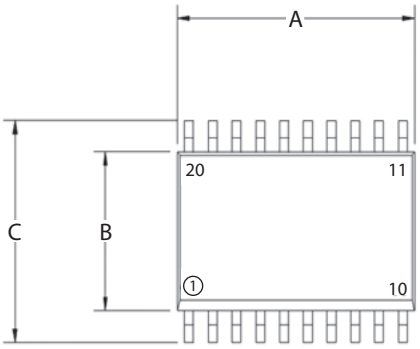
4.2 Applications Information

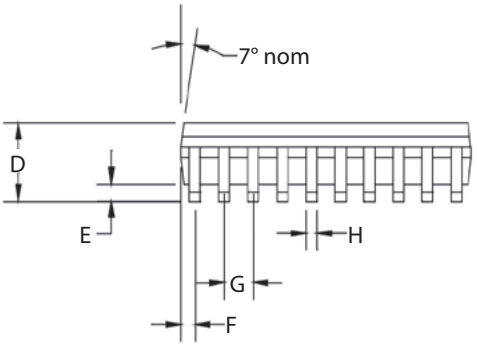
Note: The V1401 accepts input from an ADC then outputs data in the ADAT Optical format on the optical transmitters.

5. Package Dimensions (Unit: mm)

5.1 Package Outline







5.2 Mechanical Data

Symbol	Typ.	Symbol	Typ.
A	15.40	G	1.27
B	7.50	H	0.42
C	10.30	J	0.27
D	2.50	K	8.94
E	0.20	L	0.83
F	0.64		