coolaudio

# ADAT Optical Audio Data Generator and Encoder

# V1402

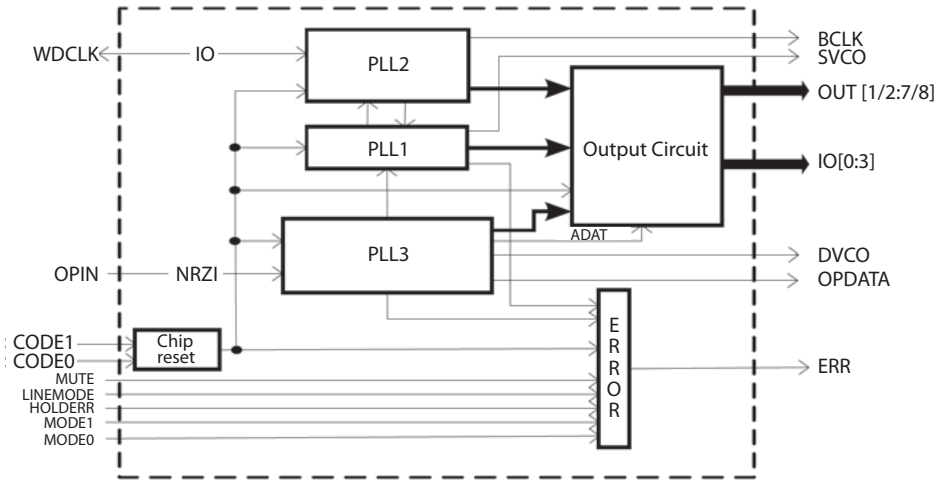
## 1. Overview

The V1402 decodes a single data stream of the industry-standard ADAT Optical protocol and produces four ADC formats stereo pairs (8 channels) of digital audio suitable for DACs or further processing. With an internal PLL to generate all needed clock signals, the V1402 requires no external clocks in Master Mode, and only word clock (Fs) for proper operation in Slave Mode. The V1402 could be applied in digital mixing boards, signal processors and sound reinforcement products, etc. V1402 features are:

- Compatible with ADAT Type I (16 bits), Type II (20 bits) and 24 bits formats
- 4 stereo pairs as outputs using standard ADC formats, supports both left and right justified data formats
- 4 IO bit outputs to receive timecode, MIDI data, S/Mux etc
- Internal PLL to generate all needed clock signals in Mater Mode
- Only word clock (Fs) for proper operation in Slave Mode
- Word clock input to synchronize outputs to user's system
- Package: SOP24

## 2. Block Diagram and Pin Description

### 2.1 Block Diagram




### 2.2 Block Description

The V1402 is consisted of chip reset, PLL3, PLL1, PLL2, ERR and output circuit. First to reset the chip before it start to work, this will reset all internal counters and state registers to their initial state and disrupt the outputs. However, PLL lock to OPIN will not be disturbed. V1402 has two work modes: Master Mode and Slave Mode. In Master Mode, the V1402 requires no external clocks. All outputs are derived from the input ADAT Optical data stream on the OPIN pin and WDCLK is an output signal. In Slave Mode, WDCLK is an input, OUT1/2-7/8, IO0-3, BCLK and SVCO are synchronous to WDCLK. Output circuit transfers the serial data to 24-bit parallel data. 8 channels of 24-bit parallel data are switched to 4 stereo pairs OUTPUT data and 4 IO data. When the V1402 lacks an input or failure to synchronize to data stream occurs, ERR is high and data outputs are muted, but not clock outputs.

### 2.2.1 General Function Descriptions

The V1402 decodes and formats a single data stream of the industry-standard ADAT Optical protocol and produces four ADC formats stereo pairs (8 channels) of digital audio suitable for DACs or further processing. The V1402 supports both ADAT Type I format (16-bit) and the ADAT Type II format (20-bit) with data lengths of up to 24 bits. IO0 is used to receive the ADAT format 32-bit timecode, IO1 is used to receive MIDI data, IO2 is used to receive the S/Mux data indicator and IO3 is reserved and should be tied low.

### 2.2.2 Mode Selection

The V1402 has two working modes, which may be selected by means of the MODE inputs. When in Master Mode, all outputs are derived from the input ADAT Optical data stream on the OPIN pin, and WDCLK is an output. In Slave Mode, OUT1/2-7/8, IO0-3, BCLK and SVCO are synchronous to WDCLK, which is an input. While in Slave mode, WDCLK may be at an arbitrary phase with respect to the incoming samples of OPIN, but if the two frequencies are not identical, samples will be dropped, repeated or garbled. Generally, identical frequencies are achieved by either using DVCO as the source from which WDCLK is generated, or by creating OPIN from a source synchronized to WDCLK.

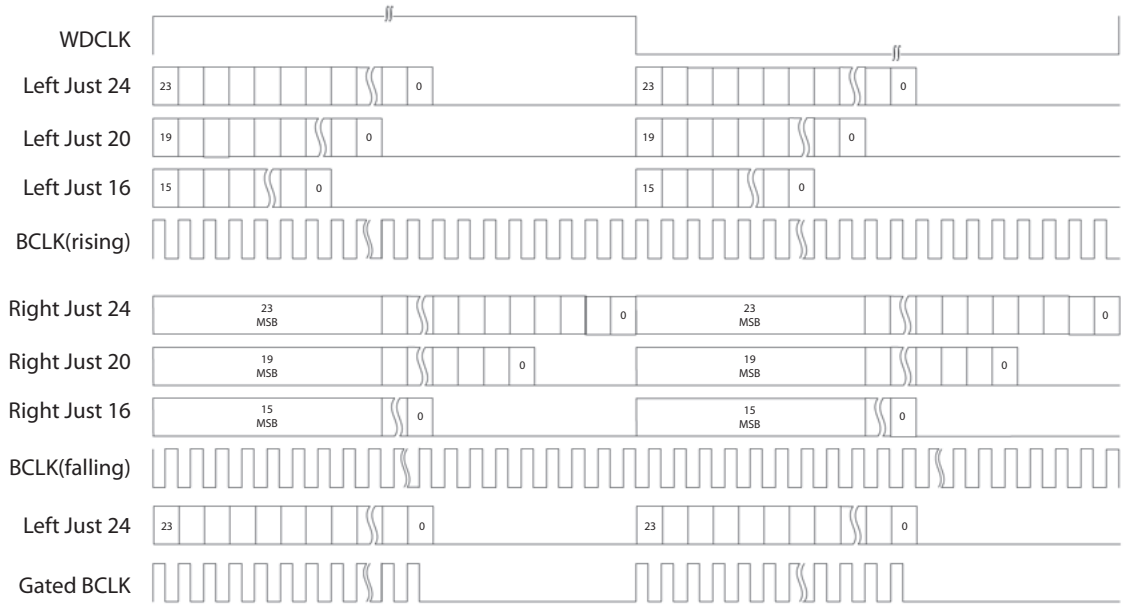
| MODE [1:0] | MODE |
|---|---|
| 00 | Master mode, WDCLK is an output |
| 01 | Slave mode, WDCLK is an input |
| 10 | Reserved |
| 11 | Reserved |

### 2.2.3 Serial Output Interface

The V1402 has been designed for ease of use and flexibility in systems interfacing with the ADAT protocol. It supports both left and right justified data formats for ease of integration into existing devices, as well as new devices. These formats allow it to operate in parallel with many standard ADCs. The specific output format to be used is selected by the format pins CODE1 and CODE0.

| CODE [1:0] | Format |
|---|---|
| 00 | Right justified, BCLK falls on WDCLK edge |
| 01 | Left justified, BCLK rises on WDCLK edge |
| 10 | Chip reset |
| 11 | Gated BCLK, BCLK rises on WCLK edge |

Serial output formats



### 2.2.4 Reset Circuitry

Reset circuitry initiated by setting CODE [1:0] = 10, is synchronous and a minimum duration of one DVCO clock period is required. At a nominal 12.288 MHz this translates to 82 ns. A safety margin is advised, and a pulse width of 100 ns would be sufficient to reset the chip. This will reset all internal counters and state registers to their initial state and disrupt the outputs.

However, PLL lock to OPIN will not be disturbed. The clock and data outputs of the V1402 are undefined after power-up until a proper data stream is well established on OPIN. The clock outputs may be running at an uncontrolled frequency during that time. In this case, the ERR pin will be high, indicating that the outputs are invalid. This can be prevented using the CODE pins to reset the V1402 on power-up, stopping the VCO clocks and muting the data output. The CODE pins may then be set to the value required in your system. Nevertheless, the V1402 will synchronize and produce proper outputs when proper and valid inputs are provided, whether this reset procedure is used or not.

### 2.2.5 Inner PLL

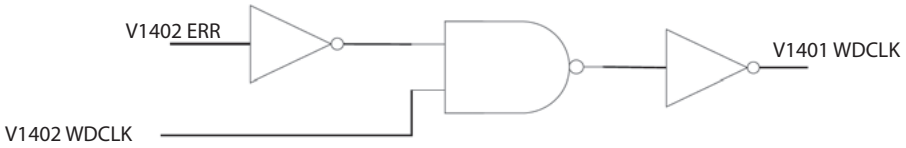
The V1402 contains an internal PLL that locks to the embedded clock in the ADAT Optical data stream and produces all necessary high frequency clocks and timing signals to operate the device. This high quality PLL will reject any high-frequency jitter on the incoming data stream. Using the extracted clock, the PLL generates the DVCO output. The data stream is also reconstructed using this PLL and output on OPDATA (clocked on the rising edge of DVCO), and thus the OPDATA data stream is synchronized to the PLL's word clock, as well as to OPIN.

The V1402 contains a duplicate PLL that locks to the incoming clock signal on WDCLK when in slave mode. Receiving 8 channels of ADAT Optical data on OPIN, the jitter was measured to be 1.26 ns typical on BCLK.

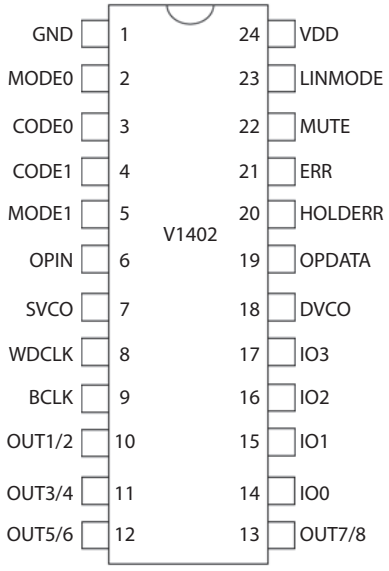
The second PLL locks onto the word clock selected by the user via the Master/Slave Mode selection. In Master Mode, the selected word clock comes from the first PLL, SVCO, BCLK and WDCLK, and all are synchronized to it. In Slave Mode, WDCLK is an input, and is what SVCO and BCLK are locked to.

### 2.2.6 Word Clock Muting

The V1402 in Master Mode can produce clock outputs running at uncontrolled frequencies, if the digital input becomes unstable after stable use. This occurs mainly due to poor connection of the optical cable to the optical connector. Care should be taken when running the V1402 with the DAC, as it will output noise if the WDCLK is operated at an uncontrolled VCO frequency beyond the DAC's maximum. An external AND gate implementation may be used to correct this. The inverted ERR pin and the desired V1402 output clock are inputs to the AND gate and the desired mutable clock is the output, and the AND function will mute the selected V1402 clock when the ERR pin is high (i.e. when unstable input is present at OPIN). In place of this circuit, the ERR pin may be used as a mute select for any audio output stage muting circuitry that is present in the system.



## 2.3 Pin Configuration



## 2.4 Pin Description

| Pin | Symbol | Function | Attribute |
|---|---|---|---|
| 1 | GND | Grand connection | Grand |
| 2 | MODE0 | Mode 0, sets mode | I |
| 3 | CODE0 | Code 0, sets data format | I |
| 4 | CODE1 | Code 1, sets data format | I |
| 5 | MODE1 | Mode 1, set mode | I |
| 6 | OPIN | Input to optical receiver | I |
| 7 | SVCO | Slave mode: WDCLK-derived clock<br>Master mode: DVCO-derived clock<br>(normal 12.288 MHz, 256*Fs) | O |
| 8 | WDCLK | Slave mode: word clock input<br>Master mode: word clock output<br>(normal 48 kHz, Fs) | I/O |
| 9 | BCLK | Bit-clock output (normal 3.072 MHz, 64 ☒ Fs) | O |
| 10 | OUT1/2 | Channel 1 & 2 data output | O |
| 11 | OUT3/4 | Channel 3 & 4 data output | O |
| 12 | OUT5/6 | Channel 5 & 6 data output | O |
| 13 | OUT7/8 | Channel 7 & 8 data output | O |
| 14 | IO0 | IO 0 data-bit output, used to receive timecode | O |
| 15 | IO1 | IO 1 data-bit output, used to receive MIDI data | O |
| 16 | IO2 | IO 2 data output, used to receive S/Mux indicator | O |
| 17 | IO3 | IO 3 data output, reserved | O |
| 18 | DVCO | Recovered clock from data stream<br>(normal 12.288 MHz, 256 ☒ Fs) | O |
| 19 | OPDATA | Regenerated OPIN for daisy-chaining | O |
| 20 | HOLDERR | If high, ERR pin stays high until cause of ERR<br>removed and HOLDERR goes low | I |
| 21 | ERR | Indicates lack of input or failure to synchronize to data stream<br>(if high, data output muted but not clock outputs) | O |
| 22 | MUTE | Mute select: 1 = Mute output; 0 = No muting | I |
| 23 | LINMODE | Tie high | I |
| 24 | VDD | VDD power pin | Power |

## 2.5

## 3. Electrical Characteristics

### 3.1 Absolute Maximum Ratings

Unless otherwise specified, Tamb = 25°C

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 ~ 4.0 | V |
| Input/Output Voltage | $V_{IN}$ / $V_{OUT}$ | GND – 0.3 ~ $V_{DD}$ + 0.3 | mA |
| Operating Temperature | $T_{amb}$ | 0 ~ 70 | °C |
| Storage Temperature | $T_{stg}$ | -65 ~ 150 | °C |

### 3.2 Electrical Characteristics

#### 3.2.1 DC Parameter

Unless otherwise specified, $T_{amb}$ = 25°C

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 4.5 | 5.0 | 5.5 | V |
| Supply current, master | $I_{DD}$ Master | — | 7.7 | — | mA |
| Supply current, slave | $I_{DD}$ Slave | — | 5.4 | — | mA |
| Ground | GND | — | 0.0 | — | V |
| Sample rate | Fs | 30 | 48 | 55 | kHz |
| Temperature | Temp | 0 | 25 | 70 | °C |
| Inputs (WDCLK, CODE, OPIN, MODE, LINMODE, MUTE, HOLDERR) | | | | | |
| Logical “1” input voltage | $V_{IH}$ | 0.75 VDD | — | — | $V_{DD}$ |
| Logical “0” input voltage | $V_{IL}$ | — | — | 0.25 VDD | $V_{DD}$ |
| Logical “1” input current | $I_{IH}$ | — | — | 1 | µA |
| Logical “0” input current | $I_{IL}$ | — | — | 1 | µA |
| Logical input capacitance | $C_{IN}$ | — | | 1 | pF |
| Outputs (WDCLK, DVCO, OPDATA, SVCO, BCLK) | | | | | |
| Logical “1” output voltage | $V_{OH}$ | 0.9 VDD | — | — | $V_{DD}$ |
| Logical “0” output voltage | $V_{OL}$ | — | — | 0.1 VDD | $V_{DD}$ |
| Logical “1” output current | $I_{OH}$ | — | — | -8 | mA |
| Logical “0” output current | $I_{OL}$ | — | — | 8 | mA |
| Outputs (OUT, IO, ERR) | | | | | |
| Logical “1” output voltage | $V_{OH}$ | 0.9 VDD | — | — | $V_{DD}$ |
| Logical “0” output voltage | $V_{OL}$ | — | — | 0.1 VDD | $V_{DD}$ |
| Logical “1” output current | $I_{OH}$ | — | — | -2 | mA |
| Logical “0” output current | $I_{OL}$ | — | — | 2 | mA |

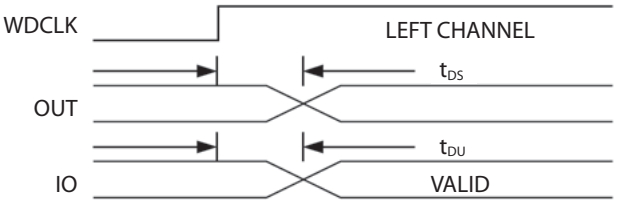
### 3.2.2 AC Parameter

Unless otherwise specified, $T_{amb}$ = 25°C

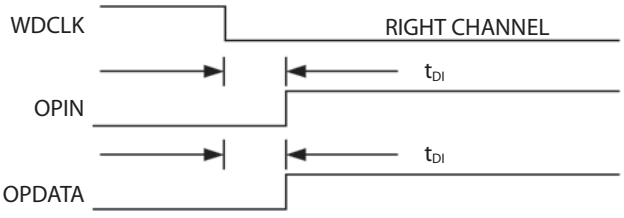
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| OUT setup time relative to Master WDCLK output | $t_{DS(Mstr)}$ | -10 | 2 | 27 | ns |
| OUT setup time relative to Slave WDCLK input | $t_{DS(Slav)}$ | -7 | 5 | 30 | ns |
| IO setup time relative to Master WDCLK output | $t_{DU(Mstr)}$ | -10 | 0 | 25 | ns |
| IO setup time relative to Slave WDCLK input | $t_{DU(Slav)}$ | -8 | 2 | 27 | ns |
| OPIN setup time relative to Master WDCLK output | $t_{DI}$ | -34 | -53 | -72 | ns |
| OPDATA setup time relative to Master WDCLK output | $t_{DT}$ | -20 | -4 | 5 | ns |
| BCLK setup time relative to Slave WDCLK output | $t_{DB}$ | 0 | 9 | 30 | ns |

Note: Above specifications hold after 3900 WDCLK cycles of valid input at OPIN.

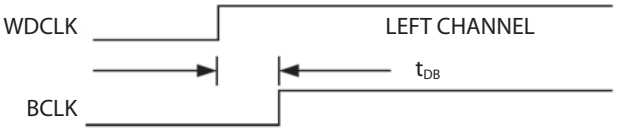
Serial Output Training




Master Mode Timing

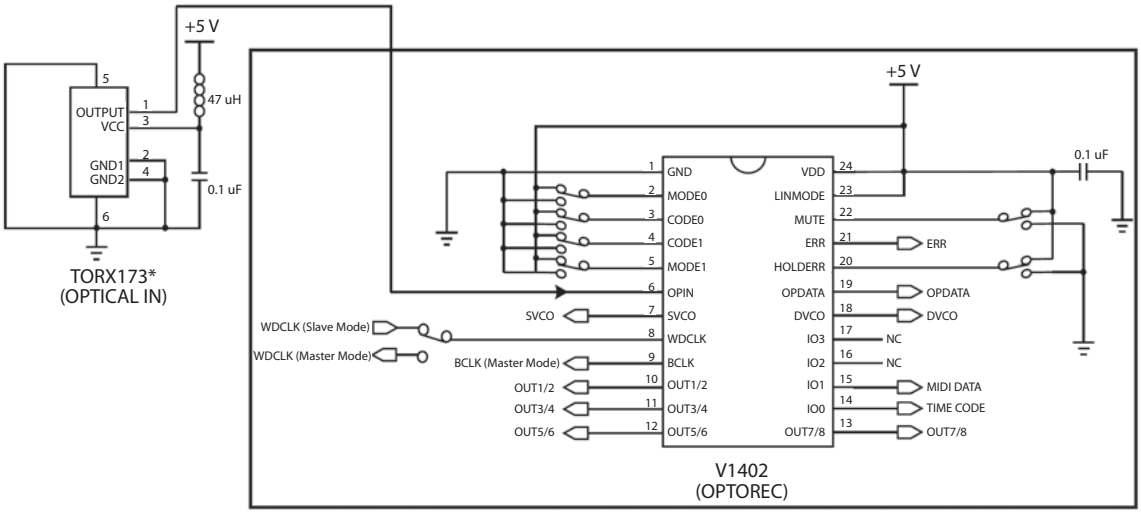



Slave Mode Timing



## 4. Typical Application Circuit and Information

### 4.1 Application Circuit

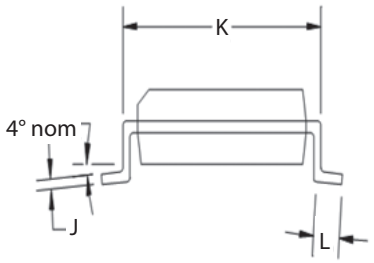


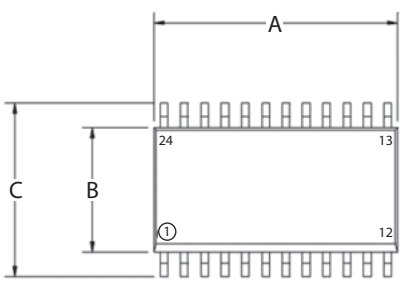

### 4.2 Applications Information

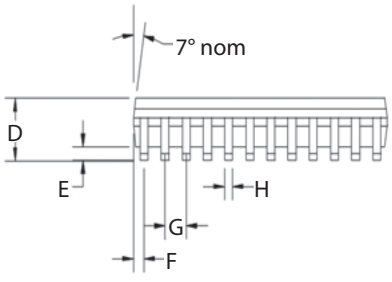
Note: The V1402 receives ADAT Optical data on the optical receivers then outputs data to a DAC.

## 5. Package Dimensions (Unit: mm)

### 5.1 Package Outline

## 5.2 Mechanical Data

| Symbol | Typ. | Symbol | Typ. |
|---|---|---|---|
| A | 15.40 | G | 1.27 |
| B | 7.50 | H | 0.42 |
| C | 10.30 | J | 0.27 |
| D | 2.50 | K | 8.94 |
| E | 0.20 | L | 0.83 |
| F | 0.64 | | |