V4220M

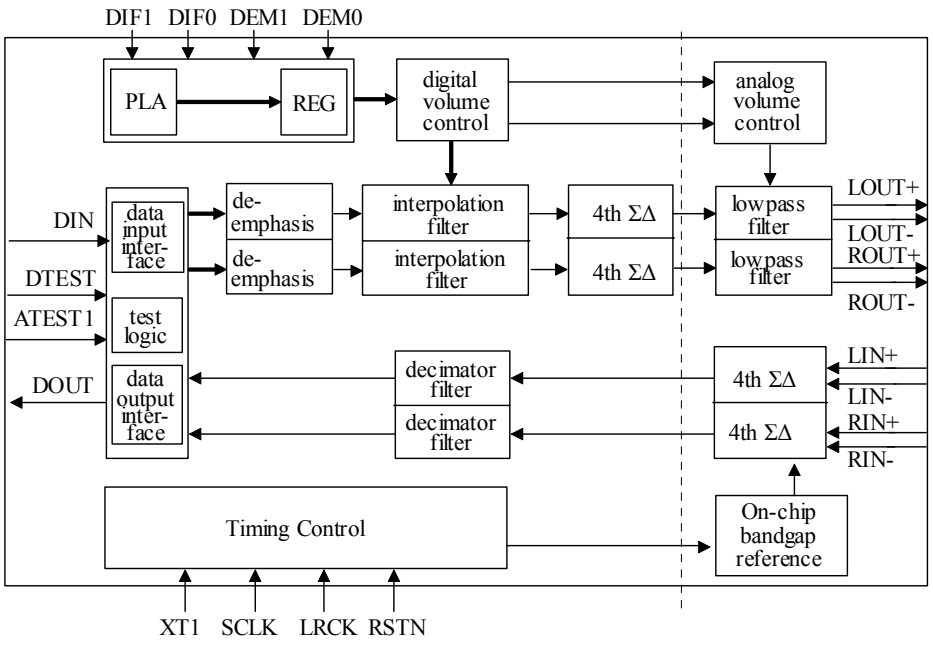
Overview

V4220M is a high performance audio codec IC using delta-sigma ADC and DAC techniques， its applications include digital effects processors, DAT, and multitrack recorders.

Its **features** are:

- 100dB dynamic range A/D converters
- 100dB dynamic range D/A converters
- 105dB DAC signal-to-noise ratio
- Analog Volume Control
- Differential inputs / outputs
- On-chip Anti-aliasing and Output Smoothing Filters
- Selectable De-emphasis Filters for 32k, 44.1k and 48kHz sample rates
- Package：SSOP28

Block Diagram and Pin Description

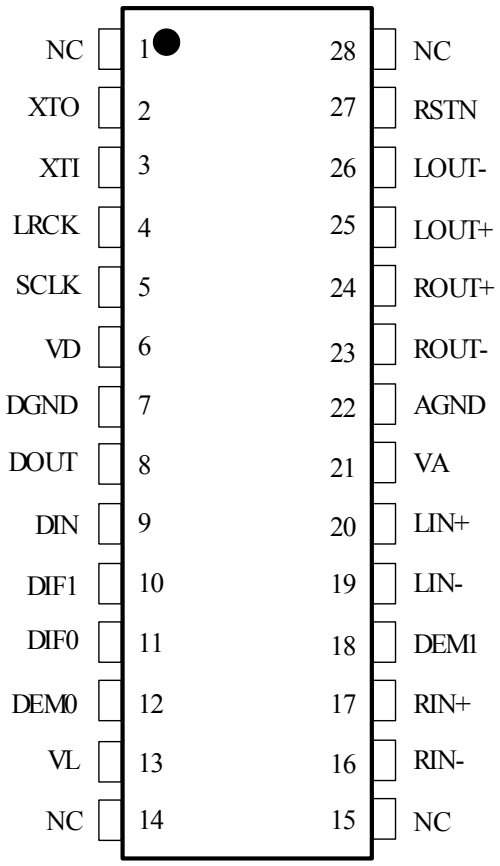


Function Description

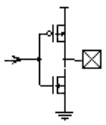
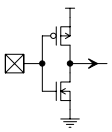
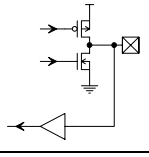
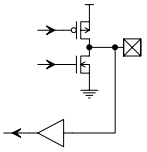
V4220M is a high performance, 24-bit, stereo, audio codec IC that includes two channel ADC and two channel DAC. The fourth-order delta-sigma A/D converters the analog input to the 24bit serial outputs; the delta-sigma DAC includes the interpolation filter, noise shaping modulator and low-pass smoothing filter.

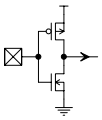
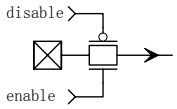
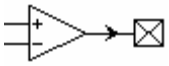
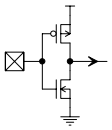
The V4220M also includes a digital selectable de-emphasis filter for 32k, 44.1k and 48k Hz sample rates; an analog volume control architecture can make an 113.5dB attenuation in 0.5dB steps, which preserves dynamic range during attenuation. The V4220M provides a serial interface to read/write the internal registers.

Pin Configuration



Pin Description and Structure Scheme

Pin	Symbol	Function	Attribute	Structure Scheme
1	NC	/	/	/
2	XTO	OSC Input/output	I/O	
3	XTI		I/O	
4	LRCK	Left/right clock	I/O	
5	SCLK	Serial data clock	I/O	
6	VD	Digital power		
7	DGND	Digital ground		
8	DOUT	Serial data output	I/O	
9	DIN	Serial data input	I/O	
10	DIF1 (scl/cclk)	Digital interface format	I	

11	DIF0 (sda/cdin)		I/O	
12	DEM0(ad0/cs)	De-emphasis select	I	
18	DEM1(I^2C/SPI)			
13	VL	Digital logic power		
14,15	NC	/	/	
16	RIN-	Differential right channel analog input	I	
17	RIN+			
19	LIN-	Differential left channel analog input	I	
20	LIN+			
21	VA	Analog power		
22	AGND	Analog ground		
23	ROUT-	Differential right channel analog output	I/O	
24	ROUT+			
25	LOUT+	Differential left channel analog output	I/O	
26	LOUT-			
27	RSTN	Reset	I	
28	NC	/	/	

Electrical Characteristics

- **Absolute Maximum Ratings**

Unless otherwise specified，T_{amb}= 25℃

Parameter	Symbol	Value	Unit
Power Supplies	V_A,V_D,V_L	-0.3～6	V
Power Supply Current	I_{all}	90	mA
Power Dissipation	P_D	450	mW
Operating Temperature	T_{amb}	-40～85	℃
Storage Temperature	T_{stg}	-65～+150	℃

- **Recommended Operating Conditions**

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Digital power	VD	4.75	5.0	5.25	V
Analog power	VA	4.75	5.0	5.25	V
Digital power	VL	2.7	5.0	5.25	V

- **Electrical Characteristics**

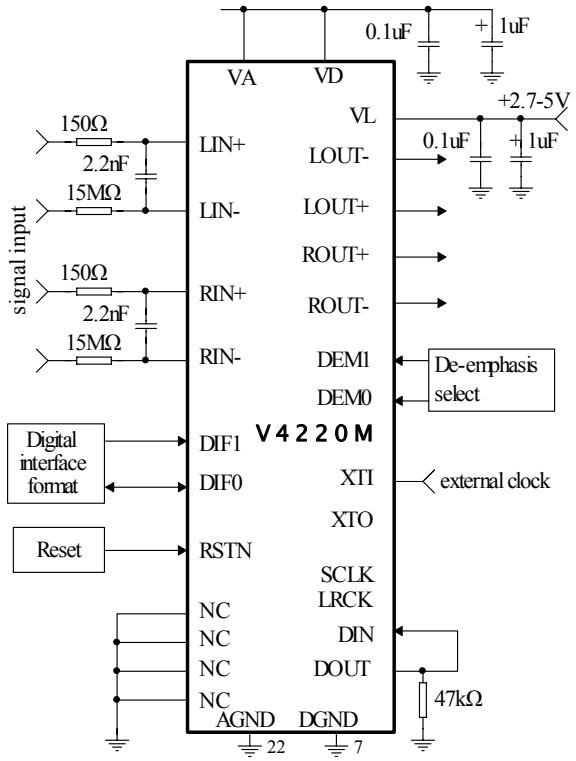
Unless otherwise specified, T_{amb}= 25℃, V_A=V_D=5V

Parameter	Symbol	Test Conditions /Comments	Specifications			Unit
			Min	Typ	max	
DC Parameter						
Power supply Current						
VA	Iva	V_L=5V		46	60	mA
VD	Ivd	V_L=5V		9	20	mA
VL	Ivl	V_L=5V		3	5	mA
Analog input characteristics						
Total harmonic distortion	THD			0.003		%
ADC dynamic range			92	100	-	dB
Total harmonic distortion +noise	THD＋N	Note 1		-92	-87	dB
Full scale input voltage		Differential		2.0	2.1	Vrms
Analog output characteristics						
Total harmonic distortion	THD			0.003		%
DAC dynamic range			92	100	-	dB
DAC SNR	SNR		97	105		dB
Attenuation step size			0.35	0.5	0.65	dB
Common mode output voltage				2.4		V
Digital characteristics						
High-level input voltage	Vih	VL=5V	2.8		VL+0.3	V
	Vil	VL=3V	2.0		VL+0.3	V
Low-level input voltage	Vil		-0.3		0.8	V
High-level output voltage			Vl-1			V
Low-level out voltage					0.5	V
Input leakage current		Logic Inputs			10	μA
Output leakage current		High Impedance Logic Outputs			10	μA

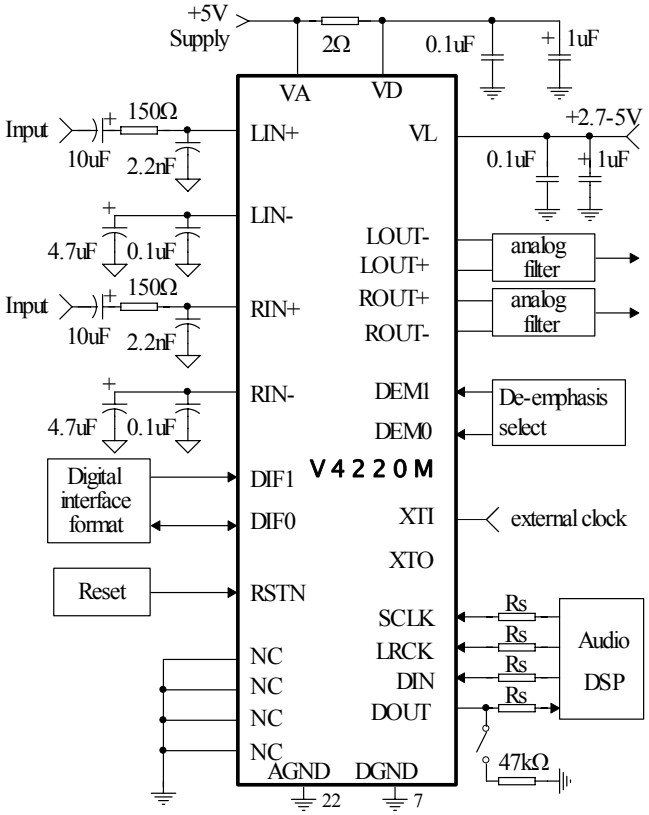
Note 1: referenced to typical full-scale differential input voltage(2 Vrms)

Test Circuit

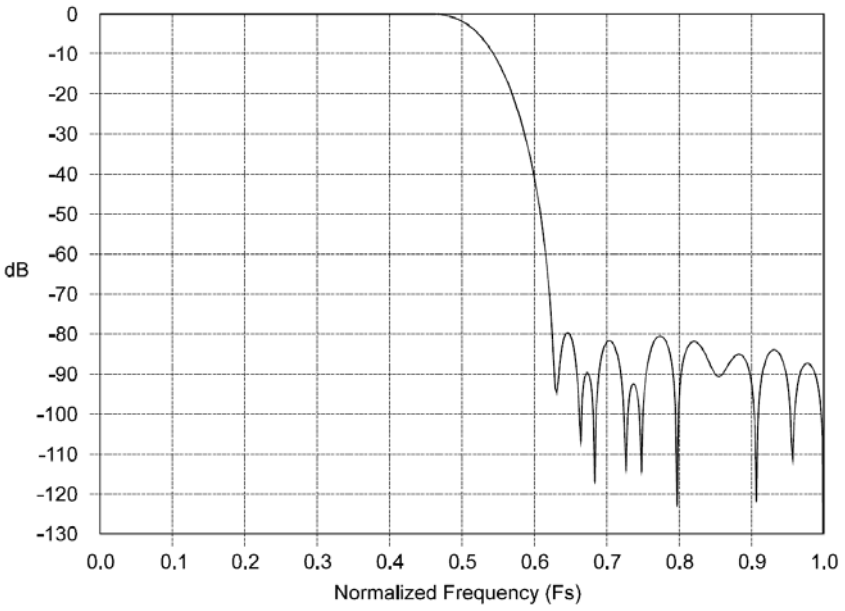
- **DC Test Circuit**



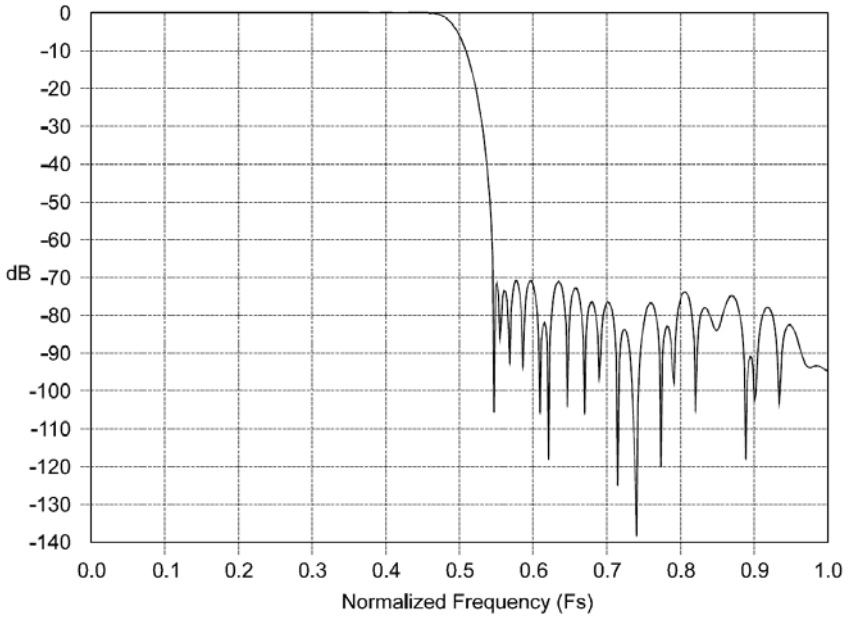
- **AC Test Circuit**



Characteristics Curve



ADC Filter Response



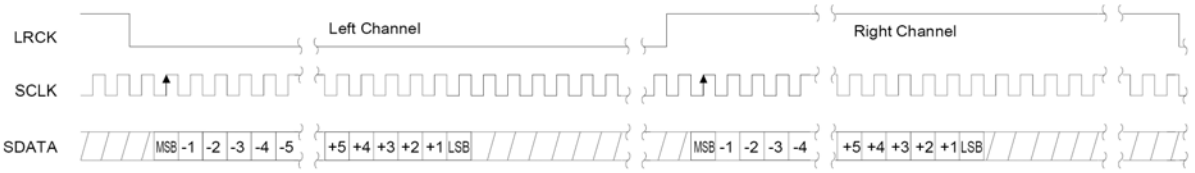
DAC Filter Response

Timing Sequence and Port Operating Description

- **digital interface format**

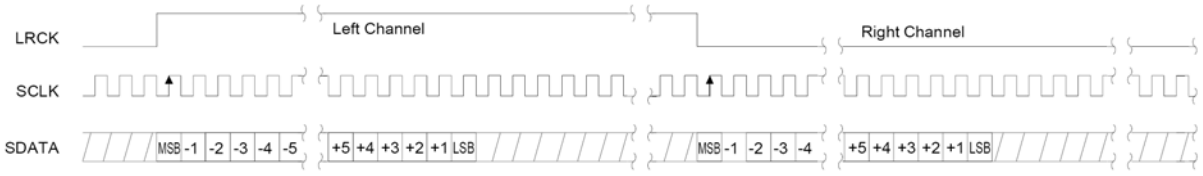
DIF1 DIF0	Digital Interface Format (Input)
00(default)	Format 1：I^2S，up to 24-bit data
01	Format 2：Left justified，up to 24-bit data
10	Format 3：Right justified，24-bit Data
11	Format 4：Right justified，20-bit Data

Serial data format 00:



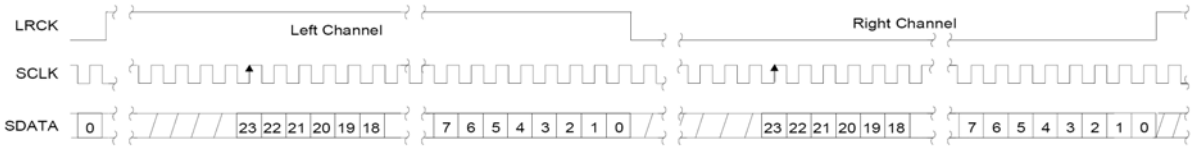
Master	Slave
I^2S, up to 24-bit data XTI=256,384,512Fs LRCK=4 to 50kHz SCLK=64Fs	I^2S, up to 24-bit data XTI=256,384,512Fs LRCK=4 to 50kHz SCLK=48,64,128Fs

Serial data format 01:



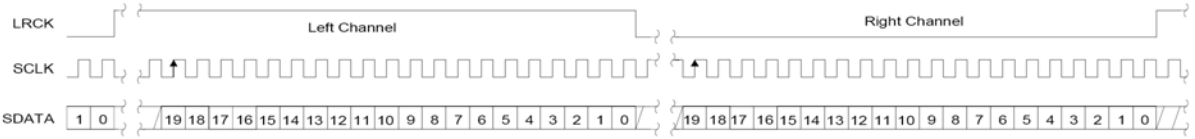
Master	Slave
Left-justified, up to 24-bit data XTI=256,384,512Fs LRCK=4 to 50kHz SCLK=64Fs	Left-justified, up to 24-bit data XTI=256,384,512Fs LRCK=4 to 50kHz SCLK=48,64,128Fs

Serial data format 10:



Master	Slave
Right-justified, 24-bit data XTI=256,384,512Fs LRCK=4 to 50kHz SCLK=64Fs	Right-justified, 24-bit data XTI=256,384,512Fs LRCK=4 to 50Hz SCLK=64Fs

Serial data format 11:



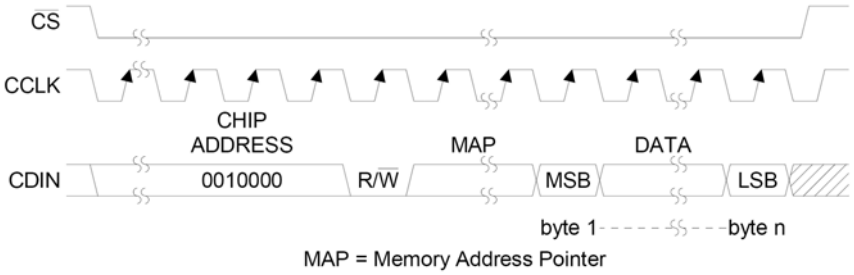
Master	Slave
Right-justified, 20-bit data XTI=256,384,512Fs LRCK=4 to 50kHz SCLK=64Fs	Right-justified, 20-bit data XTI=256,384,512Fs LRCK=4 to 50Hz SCLK=64Fs

- **Control port timing**
  - SPI mode

In SPI mode, CS is the V4220M chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the micro controller and the chip address is 0010000, all the signal are input and data is clocked in on the rising edge of CCLK.

Figure behind shows the operation of the control port in SPI mode. To write to a register, bring CS low. The first 7 bits on CDIN form the chip address, and must be 001000. The eighth bit is a read/write indicator, which must be low to write. Register reading from the V4220M is not supported in SPI model The next 8 bits form the Memory address Pointer(MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into a register designated by the MAP.

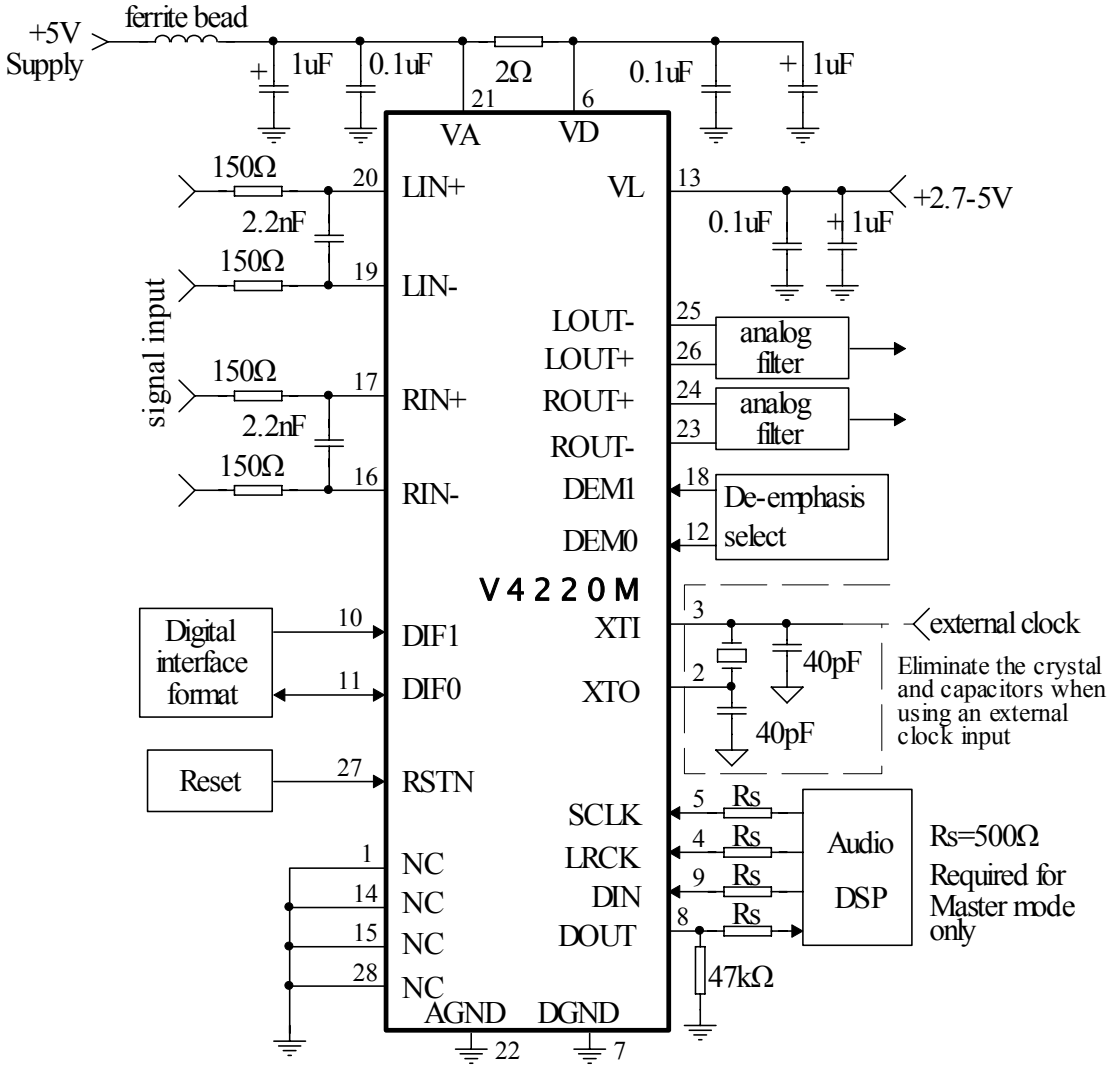
The V4220M has a MAP auto increment capability, enabled by he INCR bit in the MAP register. If INCR is a zero, then MAP will stay constant for successive writes. If INCR is set to a 1, then MAP will auto increment after each byte is written, allowing block writes of successive registers. Register reading from V4220M is not supported in the SPI mode.



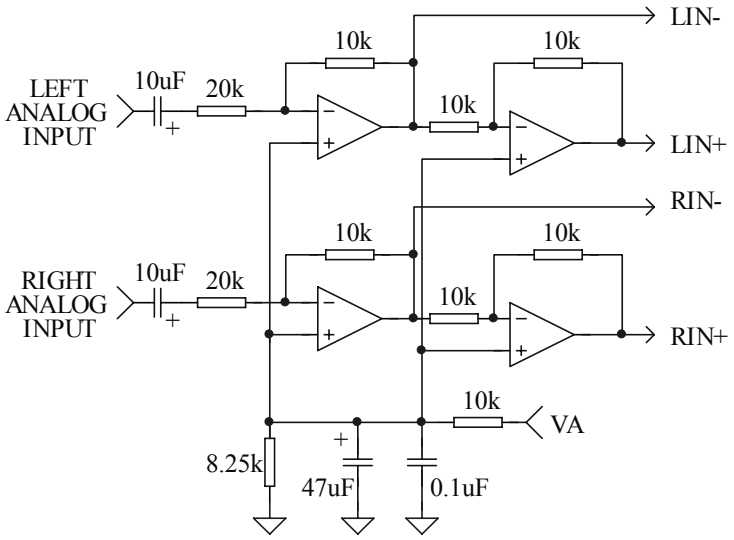
  - I^2C mode

In I^2C mode, SDA is a bi-directional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in the following figure. There is no CS pin. Pin ad0 form s the partial chip address and should be tied to VDD or DGND as desired. The upper 6 bits of the 7 bit address field must be 001000. In order to communicate with the V4220M, the LSB of the chip address field(first byte sent to the V4220M)should match the setting of the ad0 pin. The eighth bit of the address byte is the read/write bit(high for a read, low for a write). If the operation is a write, the next byte is the memory address pointer which selects the register to be read/write. If the operation is a read, the contents of the register pointed to by the memory address pointer will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

Typical Application Circuit and Information

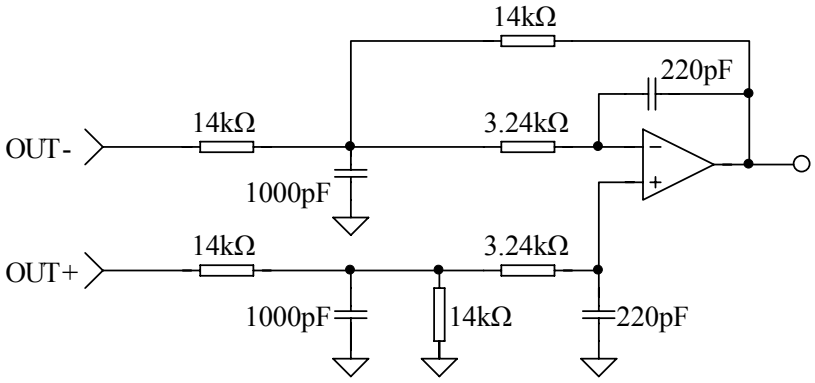


- **Input buffer**



Optional Input Buffer

- **Output buffer**



2-pole Butterworth Filter

- **Applications Information**

Master mode and slave mode:

The V4220M may be operated in either master mode or slave mode. In master mode, SCLK and LRCK are outputs which generated by inner circuit. The V4220M will operate in master mode when a 47kΩ pulldown resistor is present on DOUT at startup or after reset, see application circuit. LRCK and SCLK are inputs to the V4220M when operating in slave mode, see the available clocking modes.