OptoSupply
Light It Up

0.56 Inch Single Digit 7 Segment LED Display With CD4026B Decade Counters/Dividers

OSL10564-CD4026B-X

■ Descriptions:

CD4026B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display.

Inputs common to both types are CLOCK (CL), RESET (RS), & CLOCK INHIBIT (CD); common outputs are CARRY OUT (CO) and one digit 7 segment LED display Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input (DI), DISPLAY ENABLE out (DO) and UNGATED "C-SEGMENT" outputs (UCG).

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY OUT (Co) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs using 7 segment LED display device used for representing the decimal numbers 0 to 9. The 7 segment LED display ON when the DISPLAY ENABLE IN is high When the DISPLAY ENABLE IN is low the 7 segment LED display is OFF. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing. The CARRY OUT (CO) and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

■ Features

- 0.56 inch Single digit 7-segment LED board with Decade Counter/Dividers CD4026B
- Ideal for low-power displays. Display enable output.
- Schmitt-triggered clock inputs. Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for description of 'B' Series CMOS Devices".

■ Applications

- Decade counting
- Frequency division
- Counter/display driver for meter applications.
- Clocks, watches, timers (e.g. ÷60, ÷60, ÷12 counter/display)

■ Absolute Maximum Rating (Ta=25℃)

Item	Symbol	Value	Unit
Operating Supply Range(DC)	Vi	6	V
Input Current(DC)	Ii	45	mA
Power Dissipation	P_t	270	mW
Operating Temperature	Topr	-30 ~ +70	℃
Storage Temperature	Tstg	-40~ +85	℃
Lead Soldering Temperature(1.6mm from seating plane)	Tsol	260℃/5sec	℃

■ Electrical -Optical Characteristics (Ta=25℃)

Part Number	Color			Input Voltage(DC) Vi(V)			Input Current If(MA)	Iv(mcd)	λD(nm)/CCT(K)		
				Min.	Typ.	Max.	Max.	Typ.	Min.	Typ.	Max.
OSL10564-CD4026B-W	White	W		3	-	6	45	65	8000-18000K		
OSL10564-CD4026B-M	Warm White	M		3	-	6	45	60	2700-3300K		
OSL10564-CD4026B-B	Blue	B	■	3	-	6	45	50	460	470	475
OSL10564-CD4026B-G	Pure Green	G	■	3	-	6	45	200	515	520	530
OSL10564-CD4026B-YG	Yellow Green	YG	■	3	-	6	45	20	565	571	575
OSL10564-CD4026B-Y	Yellow	Y	■	3	-	6	45	60	585	590	595
OSL10564-CD4026B-R	Red	R	■	3	-	6	45	100	620	625	630

*1 Tolerance of measurements of chromaticity coordinates is ±10%
*2 Tolerance of measurements of dominant wavelength is ±1nm
*3 Tolerance of measurements of luminous intensity is ±15%
*4 Tolerance of measurements of forward voltage is ±0.1V

LED & Application Technologies

ISO 9001: 2008

ATTENTION
OBSERVE PRECAUTIONS
ELECTROSTATIC
SENSITIVE DEVICES

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■ Package Dimensions and Pin Function

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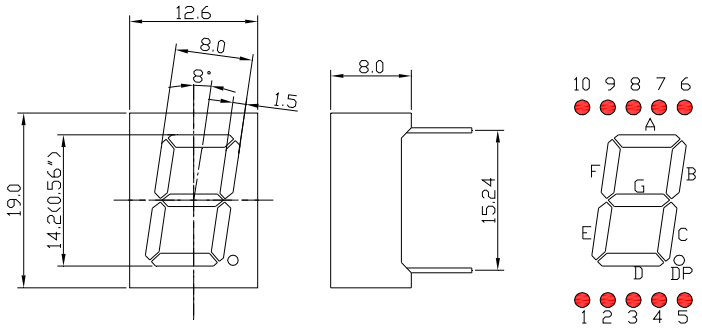
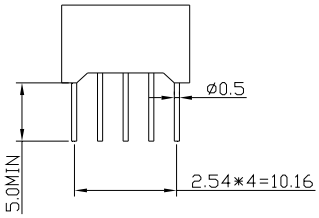
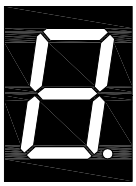


Note:

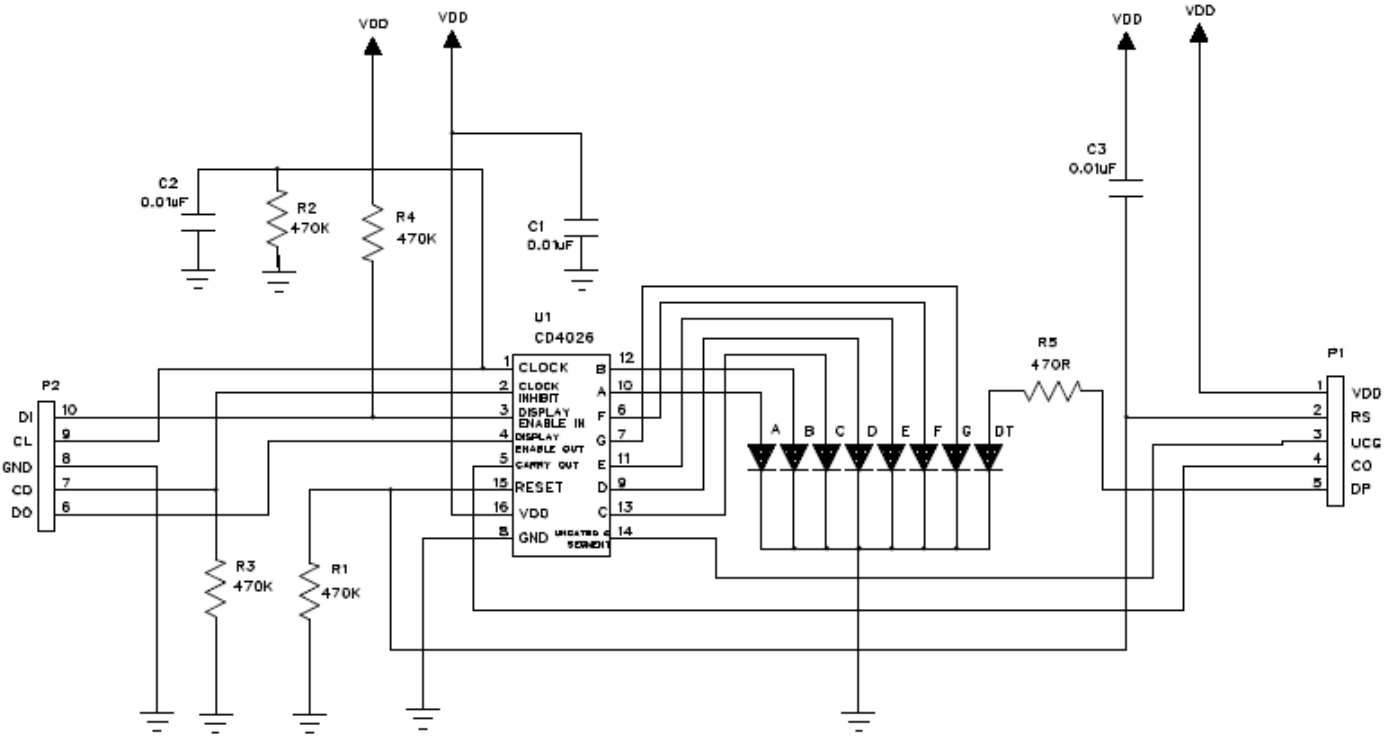
1,Unit : mm(Tolerance:±0.25mm unless otherwise noted)

2, The slope angle of any PIN may be±5.0°Max



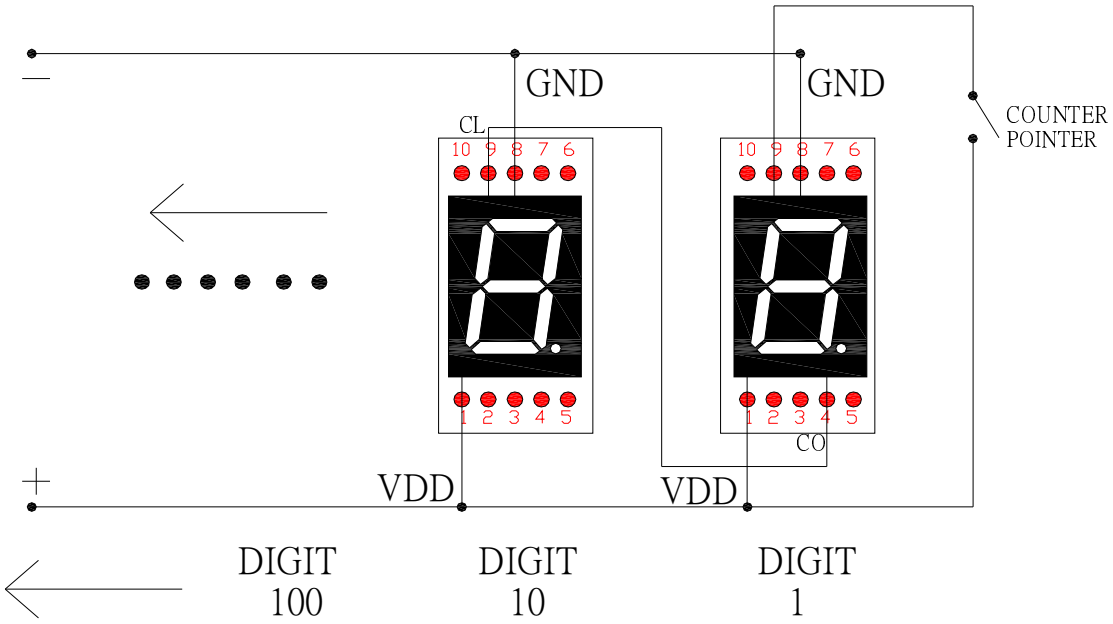


3. Circuit diagram

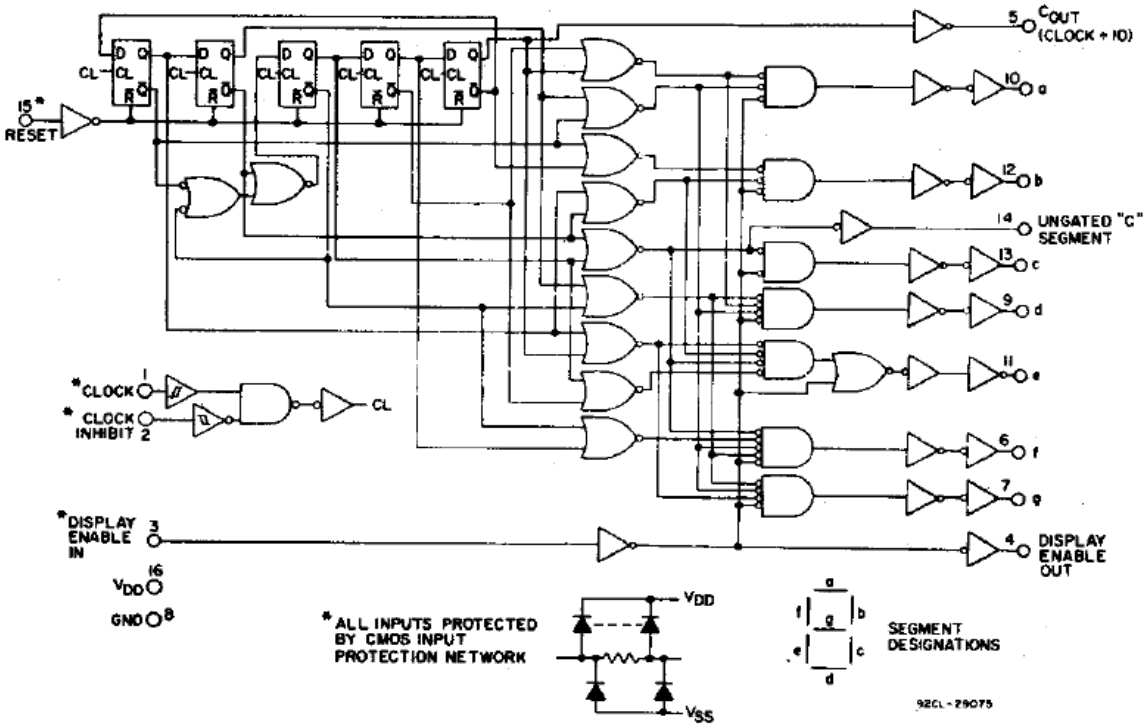


■Applications

PIN	SYMBOL	DESCRIGTION
1	VDD	VDD
2	RS	RESET
3	UCG	UNGATED "C-SEGMENT"
4	CO	CARRY OUT
5	DP	DOT POINT
6	DO	DISPLAY ENABLE OUT
7	CD	CLOCK INHIBIT
8	GND	GND
9	CL	CLOCK
10	DI	DISPLAY ENABLE IN



4. CD4026B logic diagram :



5. CD4026B timing diagram :