BUILT-IN DELAY CIRCUIT HIGH-PRECISION VOLTAGE DETECTOR **S-809 Series**

The S-809 Series is a high-precision voltage detector developed using CMOS process. The detection voltage is fixed internally, with an accuracy of ±2.0%. Attachment of an external capacitor can delay the release signal. Two output types, Nch open-drain and CMOS output, are available.

■ Features

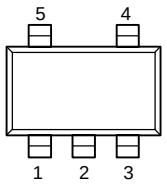
- Ultra-low current consumption
  1.0 µA typ. (V_{DD}=2.0 V)
  ; Products with a detection voltage of 1.4 V or less
  1.2 µA typ. (V_{DD}=3.5 V)
  ; Products with a detection voltage of 1.5 V or more
- High-precision detection voltage
  ±2.0%
- Low operating voltage
  0.80 to 6.0 V
  ; Products with detection voltage of 1.4 V or less
  0.95 to 10.0 V
  ; Products with detection voltage of 1.5 V or more
- Hysteresis characteristics
  5% typ
- Detection voltage
  1.1 to 6.0 V
  (0.1V step)
- Nch open-drain active low and CMOS active low output
- SOT-23-5 Very-small plastic package

■ Applications

- Battery checker
- Power failure detector
- Power monitor for portable equipment such as pagers, electric calculators, electric notes and remote controllers
- Constant voltage power monitor for cameras, video equipment and communication devices
- Power monitor for microcomputers and reset for CPUs

■ Pin Assignment

SOT-23-5
Top view

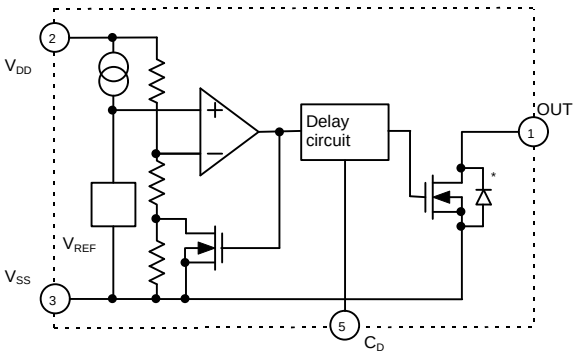


1 OUT
2 V_{DD}
3 V_{SS}
4 NC
5 C_D

Figure 1

■ Block Diagram

(1) Nch open-drain active low output



(2) CMOS active low output

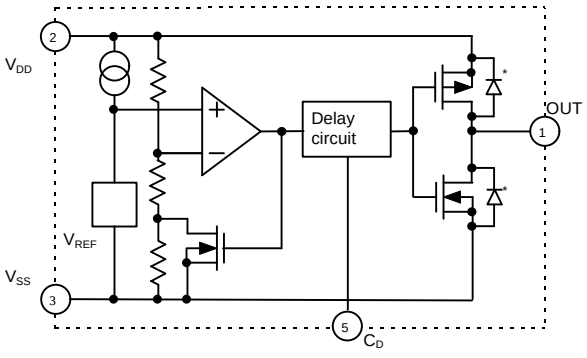


Figure 2

*Parasitic diode

■ Selection Guide

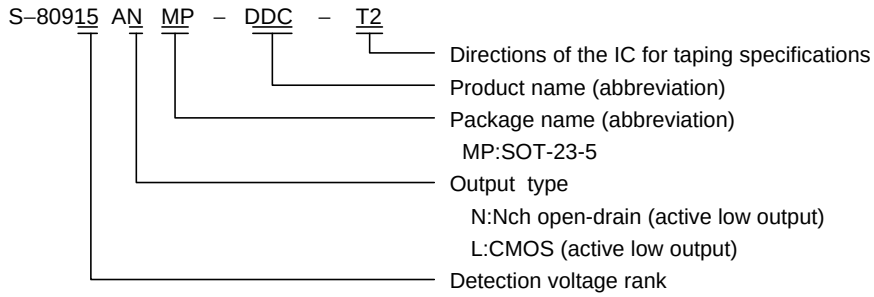


Table 1

Detection voltage range (V)	Hysteresis width V_{HYS} typ.(V)	Nch Open Drain(Low)	CMOS Output(Low)
1.1V±2.0%	0.055	S-80911ANMP-D71-T2	S-80911ALMP-D51-T2
1.2V±2.0%	0.060	S-80912ANMP-D72-T2	S-80912ALMP-D52-T2
1.3V±2.0%	0.065	S-80913ANMP-DDA-T2	S-80913ALMP-DAA-T2
1.4V±2.0%	0.070	S-80914ANMP-DDB-T2	S-80914ALMP-DAB-T2
1.5V±2.0%	0.075	S-80915ANMP-DDC-T2	S-80915ALMP-DAC-T2
1.6V±2.0%	0.080	S-80916ANMP-DDD-T2	S-80916ALMP-DAD-T2
1.7V±2.0%	0.085	S-80917ANMP-DDE-T2	S-80917ALMP-DAE-T2
1.8V±2.0%	0.090	S-80918ANMP-DDF-T2	S-80918ALMP-DAF-T2
1.9V±2.0%	0.095	S-80919ANMP-DDG-T2	S-80919ALMP-DAG-T2
2.0V±2.0%	0.100	S-80920ANMP-DDH-T2	S-80920ALMP-DAH-T2
2.1V±2.0%	0.105	S-80921ANMP-DDJ-T2	S-80921ALMP-DAJ-T2
2.2V±2.0%	0.110	S-80922ANMP-DDK-T2	S-80922ALMP-DAK-T2
2.3V±2.0%	0.115	S-80923ANMP-DDL-T2	S-80923ALMP-DAL-T2
2.4V±2.0%	0.120	S-80924ANMP-DDM-T2	S-80924ALMP-DAM-T2
2.5V±2.0%	0.125	S-80925ANMP-DDN-T2	S-80925ALMP-DAN-T2
2.6V±2.0%	0.130	S-80926ANMP-DDP-T2	S-80926ALMP-DAP-T2
2.7V±2.0%	0.135	S-80927ANMP-DDQ-T2	S-80927ALMP-DAQ-T2
2.8V±2.0%	0.140	S-80928ANMP-DDR-T2	S-80928ALMP-DAR-T2
2.9V±2.0%	0.145	S-80929ANMP-DDS-T2	S-80929ALMP-DAS-T2
3.0V±2.0%	0.150	S-80930ANMP-DDT-T2	S-80930ALMP-DAT-T2
3.1V±2.0%	0.155	S-80931ANMP-DDV-T2	S-80931ALMP-DAV-T2
3.2V±2.0%	0.160	S-80932ANMP-DDW-T2	S-80932ALMP-DAW-T2
3.3V±2.0%	0.165	S-80933ANMP-DDX-T2	S-80933ALMP-DAX-T2
3.4V±2.0%	0.170	S-80934ANMP-DDY-T2	S-80934ALMP-DAY-T2
3.5V±2.0%	0.175	S-80935ANMP-DDZ-T2	S-80935ALMP-DAZ-T2
3.6V±2.0%	0.180	S-80936ANMP-DD0-T2	S-80936ALMP-DA0-T2
3.7V±2.0%	0.185	S-80937ANMP-DD1-T2	S-80937ALMP-DA1-T2
3.8V±2.0%	0.190	S-80938ANMP-DD2-T2	S-80938ALMP-DA2-T2
3.9V±2.0%	0.195	S-80939ANMP-DD3-T2	S-80939ALMP-DA3-T2
4.0V±2.0%	0.200	S-80940ANMP-DD4-T2	S-80940ALMP-DA4-T2
4.1V±2.0%	0.205	S-80941ANMP-DD5-T2	S-80941ALMP-DA5-T2
4.2V±2.0%	0.210	S-80942ANMP-DD6-T2	S-80942ALMP-DA6-T2
4.3V±2.0%	0.215	S-80943ANMP-DD7-T2	S-80943ALMP-DA7-T2
4.4V±2.0%	0.220	S-80944ANMP-DD8-T2	S-80944ALMP-DA8-T2
4.5V±2.0%	0.225	S-80945ANMP-DD9-T2	S-80945ALMP-DA9-T2
4.6V±2.0%	0.230	S-80946ANMP-DJA-T2	S-80946ALMP-DEA-T2
4.7V±2.0%	0.235	S-80947ANMP-DJB-T2	S-80947ALMP-DEB-T2
4.8V±2.0%	0.240	S-80948ANMP-DJC-T2	S-80948ALMP-DEC-T2
4.9V±2.0%	0.245	S-80949ANMP-DJD-T2	S-80949ALMP-DED-T2
5.0V±2.0%	0.250	S-80950ANMP-DJE-T2	S-80950ALMP-DEE-T2
5.1V±2.0%	0.255	S-80951ANMP-DJF-T2	S-80951ALMP-DEF-T2
5.2V±2.0%	0.260	S-80952ANMP-DJG-T2	S-80952ALMP-DEG-T2
5.3V±2.0%	0.265	S-80953ANMP-DJH-T2	S-80953ALMP-DEH-T2
5.4V±2.0%	0.270	S-80954ANMP-DJJ-T2	S-80954ALMP-DEJ-T2
5.5V±2.0%	0.275	S-80955ANMP-DJK-T2	S-80955ALMP-DEK-T2
5.6V±2.0%	0.280	S-80956ANMP-DJL-T2	S-80956ALMP-DEL-T2
5.7V±2.0%	0.285	S-80957ANMP-DJM-T2	S-80957ALMP-DEM-T2
5.8V±2.0%	0.290	S-80958ANMP-DJN-T2	S-80958ALMP-DEN-T2
5.9V±2.0%	0.295	S-80959ANMP-DJP-T2	S-80959ALMP-DEP-T2
6.0V±2.0%	0.300	S-80960ANMP-DJQ-T2	S-80960ALMP-DEQ-T2

■ Output Configurations

1. S-809 Series model numbering system

	Nch open-drain ("L" reset type)	CMOS output ("L" reset type)
S-809 Series	"N" is the last letter of the model number. e.g. S-80915AN	"L" is the last letter of the model number. e.g. S-80915AL

2. Output configurations and their implementation

Implementation	Nch("L")	CMOS("L")
With different power supplies	Yes	No
With active low reset CPUs	Yes	Yes
With active high reset CPUs	No	No
With voltage divider variable resistors	Yes	No

・ Example with two power supplies ・ Examples with one power supply

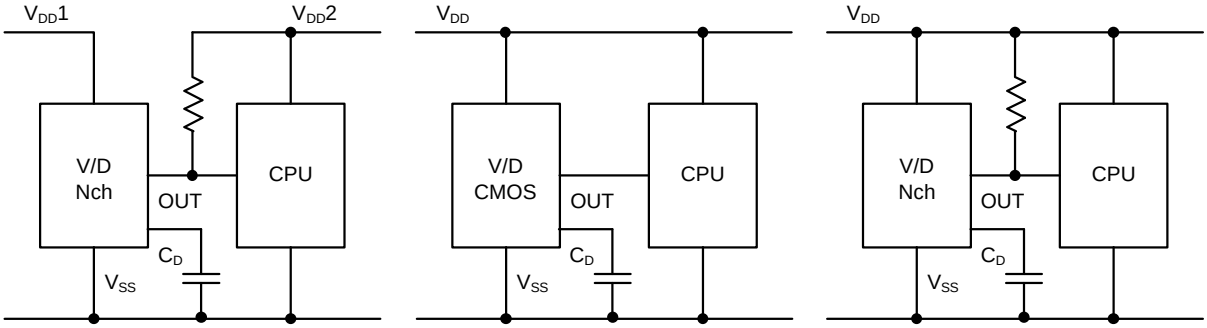


Figure 3

■ Advantage over the S-808 Series

1. Built-In delay circuit

   Delay time setting by an additional external capacitor:

   The S-809 can easily delay an release signal by attachment of an external capacitor with built-In delay circuit.

   This results in an advantage of parts reduction over the S-808 Series.

■ Absolute Maximum Ratings

1. Products with a Detection voltage of 1.4V or less.

(Unless otherwise specified: Ta=25°C)

Parameter		Symbol	Ratings	Unit
Power supply voltage		V_{DD}–V_{SS}	8	V
C^D terminal Input voltage		V_{CD}	V_{SS}-0.3 to V_{DD} +0.3	V
Output voltage	Nch open-drain	V_{OUT}	V_{SS}-0.3 to 8	V
	CMOS		V_{SS}-0.3 to V_{DD}+0.3	V
Output current		I_{OUT}	50	mA
Power dissipation		Pd	150	mW
Operating temperature		Topr	–40 to +85	°C
Storage temperature		Tstg	–40 to +125	°C

2. Products with a Detection voltage of 1.5V or more.

(Unless otherwise specified: Ta=25°C)

Parameter		Symbol	Ratings	Unit
Power supply voltage		V_{DD}–V_{SS}	12	V
C^D terminal Input voltage		V_{CD}	V_{SS}-0.3 to V_{DD} +0.3	V
Output voltage	Nch open-drain	V_{OUT}	V_{SS}-0.3 to 12	V
	CMOS		V_{SS}-0.3 to V_{DD}+0.3	V
Output current		I_{OUT}	50	mA
Power dissipation		Pd	150	mW
Operating temperature		Topr	–40 to +85	°C
Storage temperature		Tstg	–40 to +125	°C

Note: This IC has a built-in protection circuit for static electricity, however, prevent contact with a large static electricity or electrostatic voltage which exceeds the performance of the protection circuit.

■ Electrical Characteristics

1. Detection voltage (1.1V to 1.4V)

(Unless otherwise specified: Ta=25°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET}$	S-80911AXMP		1.078	1.100	1.122	V	1
		S-80912AXMP		1.176	1.200	1.224		
		S-80913AXMP		1.274	1.300	1.326		
		S-80914AXMP		1.372	1.400	1.428		
Hysteresis width	V_{HYS}			$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
Current consumption	I_{SS}	V_{DD}=2.0V		—	1.0	2.5	μA	2
Operating voltage	V_{DD}			0.8	—	6.0	V	1
Output current	I_{OUT}	Nch V_{DS}=0.5V	V_{DD}=0.95V	0.03	0.25	—	mA	3
		Pch(CMOS output) V_{DS}=0.5V	V_{DD}=4.8V	0.36	0.62	—		4
Leakage current of output transistor	I_{LEAK}	Nch(Nch open drain)	V_{DS}=6.0V V_{DD}=6.0V	—	—	0.1	μA	3
Delay time	td	V_{DD}=2.0V CD=4.7nF		2.7	3.6	4.5	ms	5
Temperature characteristic of	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=-40°C to +85°C	S-80911AXMP	—	±0.19	±0.57	mV/°C	1
			S-80912AXMP	—	±0.20	±0.60		
			S-80913AXMP	—	±0.22	±0.66		
			S-80914AXMP	—	±0.24	±0.72		

2. Detection voltage (1.5V to 2.6V)

(Unless otherwise specified: Ta=25°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET}$	S-80915AXMP		1.470	1.500	1.530	V	1
		S-80916AXMP		1.568	1.600	1.632		
		S-80917AXMP		1.666	1.700	1.734		
		S-80918AXMP		1.764	1.800	1.836		
		S-80919AXMP		1.862	1.900	1.938		
		S-80920AXMP		1.960	2.000	2.040		
		S-80921AXMP		2.058	2.100	2.142		
		S-80922AXMP		2.156	2.200	2.244		
		S-80923AXMP		2.254	2.300	2.346		
		S-80924AXMP		2.352	2.400	2.448		
		S-80925AXMP		2.450	2.500	2.550		
		S-80926AXMP		2.548	2.600	2.652		
Hysteresis width	V_{HYS}			$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
Current consumption	I_{SS}	V_{DD}=3.5V		—	1.2	3.0	μA	2
Operating voltage	V_{DD}			0.95	—	10.0	V	1
Output current	I_{OUT}	Nch V_{DS}=0.5V	V_{DD}=1.2V	0.23	0.50	—	mA	3
		Pch(CMOS output) V_{DS}=0.5V	V_{DD}=4.8V	0.36	0.62	—		4
Leakage current of output transistor	I_{LEAK}	Nch(Nch open drain)	V_{DS}=10.0V V_{DD}=10.0V	—	—	0.1	μA	3
Delay time	td	V_{DD}=3.5V C_D=4.7nF	S-809XXANMP	20	27	34	ms	5
			S-809XXALMP	18	24	30		
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{Ta}$	Ta=-40°C to +85°C	S-80915AXMP	—	±0.18	±0.54	mV/°C	1
			S-80916AXMP	—	±0.19	±0.57		
			S-80917AXMP	—	±0.20	±0.60		
			S-80918AXMP	—	±0.21	±0.63		
			S-80919AXMP	—	±0.22	±0.66		
			S-80920AXMP	—	±0.24	±0.72		
			S-80921AXMP	—	±0.25	±0.75		
			S-80922AXMP	—	±0.26	±0.78		
			S-80923AXMP	—	±0.27	±0.81		
			S-80924AXMP	—	±0.28	±0.84		
			S-80925AXMP	—	±0.29	±0.87		
			S-80926AXMP	—	±0.31	±0.93		

3. Detection voltage (2.7V to 3.9V)

(Unless otherwise specified: Ta=25°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET}$		S-80927AXMP	2.646	2.700	2.754	V	1
			S-80928AXMP	2.744	2.800	2.856		
			S-80929AXMP	2.842	2.900	2.958		
			S-80930AXMP	2.940	3.000	3.060		
			S-80931AXMP	3.038	3.100	3.162		
			S-80932AXMP	3.136	3.200	3.264		
			S-80933AXMP	3.234	3.300	3.366		
			S-80934AXMP	3.332	3.400	3.468		
			S-80935AXMP	3.430	3.500	3.570		
			S-80936AXMP	3.528	3.600	3.672		
			S-80937AXMP	3.626	3.700	3.774		
			S-80938AXMP	3.724	3.800	3.876		
			S-80939AXMP	3.822	3.900	3.978		
Hysteresis width	V_{HYS}			$-V_{DET}$ 0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
Current consumption	I_{SS}	V_{DD}=4.5V		—	1.3	3.3	μA	2
Operating voltage	V_{DD}			0.95	—	10.0	V	1
Output current	I_{OUT}	Nch V_{DS}=0.5V	V_{DD}=1.2V	0.23	0.50	—	mA	3
			V_{DD}=2.4V	1.60	3.70	—		
		Pch(CMOS output) V_{DS}=0.5V	V_{DD}=4.8V	0.36	0.62	—		4
Leakage current of output transistor	I_{LEAK}	Nch(Nch open drain)	V_{DS}=10.0V V_{DD}=10.0V	—	—	0.1	μA	3
Delay time	td	V_{DD}=4.5V	S-809XXANMP	20	27	34	ms	5
		C_D=4.7nF	S-809XXALMP	18	24	30		
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=-40°C to +85°C	S-80927AXMP	—	±0.32	±0.96	mV/°C	1
			S-80928AXMP	—	±0.33	±0.99		
			S-80929AXMP	—	±0.34	±1.02		
			S-80930AXMP	—	±0.35	±1.05		
			S-80931AXMP	—	±0.36	±1.08		
			S-80932AXMP	—	±0.38	±1.14		
			S-80933AXMP	—	±0.39	±1.17		
			S-80934AXMP	—	±0.40	±1.20		
			S-80935AXMP	—	±0.41	±1.23		
			S-80936AXMP	—	±0.42	±1.26		
			S-80937AXMP	—	±0.44	±1.32		
			S-80938AXMP	—	±0.45	±1.35		
			S-80939AXMP	—	±0.46	±1.38		

4. Detection voltage (4.0V to 5.4V)

(Unless otherwise specified: Ta=25°C)

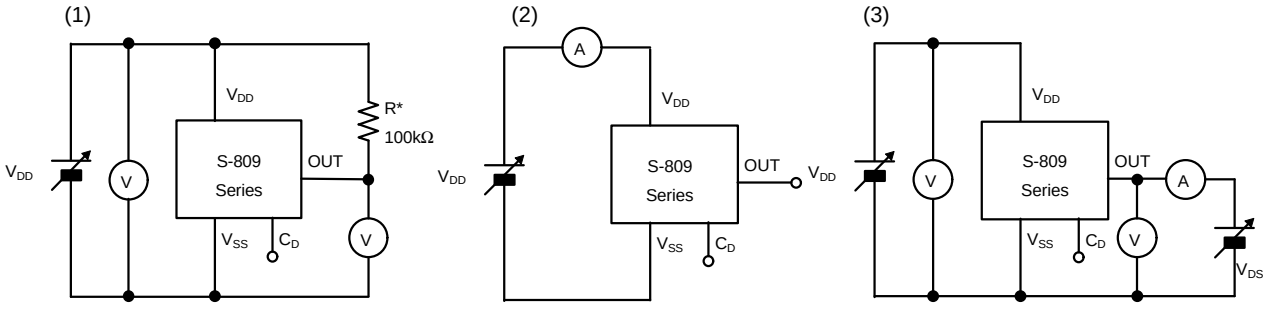
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET}$		S-80940AXMP	3.920	4.000	4.080	V	1
			S-80941AXMP	4.018	4.100	4.182		
			S-80942AXMP	4.116	4.200	4.284		
			S-80943AXMP	4.214	4.300	4.386		
			S-80944AXMP	4.312	4.400	4.488		
			S-80945AXMP	4.410	4.500	4.590		
			S-80946AXMP	4.508	4.600	4.692		
			S-80947AXMP	4.606	4.700	4.794		
			S-80948AXMP	4.704	4.800	4.896		
			S-80949AXMP	4.802	4.900	4.998		
			S-80950AXMP	4.900	5.000	5.100		
			S-80951AXMP	4.998	5.100	5.202		
			S-80952AXMP	5.096	5.200	5.304		
			S-80953AXMP	5.194	5.300	5.406		
			S-80954AXMP	5.292	5.400	5.508		
Hysteresis width	V_{HYS}			$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
Current consumption	I_{SS}	V_{DD}=6.0V		—	1.5	3.8	μA	2
Operating voltage	V_{DD}			0.95	—	10.0	V	1
Output current	I_{OUT}	Nch V_{DS}=0.5V	V_{DD}=1.2V	0.23	0.50	—	mA	3
			V_{DD}=2.4V	1.60	3.70	—		
		Pch(CMOS output) V_{DS}=0.5V	V_{DD}=6.0V	0.46	0.75	—		4
Leakage current of output transistor	I_{LEAK}	Nch(Nch open drain)	V_{DS}=10.0V V_{DD}=10.0V	—	—	0.1	μA	3
Delay time	td	V_{DD}=6.0V C_D=4.7nF	S-809XXANMP	20	27	34	ms	5
			S-809XXALMP	18	24	30		
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=-40°C to +85°C	S-80940AXMP	—	±0.47	±1.41	mV°C	1
			S-80941AXMP	—	±0.48	±1.44		
			S-80942AXMP	—	±0.49	±1.47		
			S-80943AXMP	—	±0.51	±1.53		
			S-80944AXMP	—	±0.52	±1.56		
			S-80945AXMP	—	±0.53	±1.59		
			S-80946AXMP	—	±0.54	±1.62		
			S-80947AXMP	—	±0.55	±1.65		
			S-80948AXMP	—	±0.56	±1.68		
			S-80949AXMP	—	±0.58	±1.74		
			S-80950AXMP	—	±0.59	±1.77		
			S-80951AXMP	—	±0.60	±1.80		
			S-80952AXMP	—	±0.61	±1.83		
			S-80953AXMP	—	±0.62	±1.86		
			S-80954AXMP	—	±0.64	±1.92		

5. Detection voltage (5.5V to 6.0V)

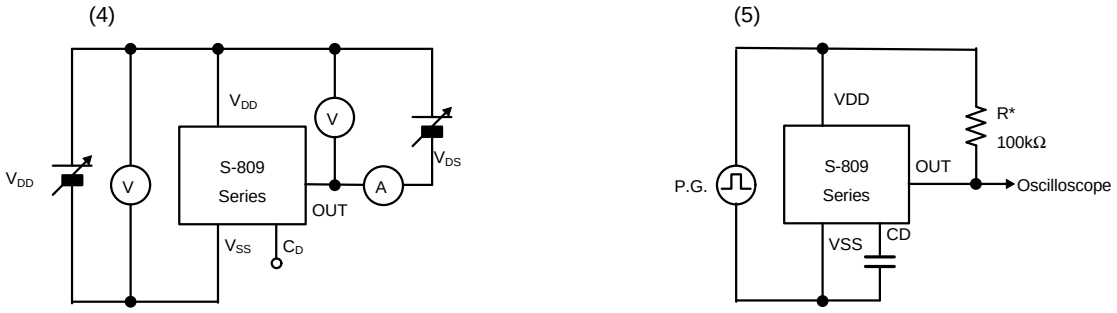
(Unless otherwise specified: Ta=25°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET}$	S-80955AXMP		5.390	5.500	5.610	V	1
		S-80956AXMP		5.488	5.600	5.712		
		S-80957AXMP		5.586	5.700	5.814		
		S-80958AXMP		5.684	5.800	5.916		
		S-80959AXMP		5.782	5.900	6.018		
		S-80960AXMP		5.880	6.000	6.120		
Hysteresis width	V_{HYS}			$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
Current consumption	I_{SS}	V_{DD}=7.5V		—	1.6	4.2	μA	2
Operating voltage	V_{DD}			0.95	—	10.0	V	1
Output current	I_{OUT}	Nch V_{DS}=0.5V	V_{DD}=1.2V	0.23	0.50	—	mA	3
			V_{DD}=2.4V	1.60	3.70	—		
		Pch(CMOS output) V_{DS}=0.5V	V_{DD}=8.4V	0.59	0.96	—		4
Leakage current of output transistor	I_{LEAK}	Nch(Nch open drain)	V_{DS}=10.0V V_{DD}=10.0V	—	—	0.1	μA	3
Delay time	td	V_{DD}=7.5V C_D=4.7nF	S-809XXANMP	20	27	34	ms	5
			S-809XXALMP	18	24	30		
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=-40°C to +85°C	S-80955AXMP	—	±0.65	±1.95	mV/°C	1
			S-80956AXMP	—	±0.66	±1.98		
			S-80957AXMP	—	±0.67	±2.01		
			S-80958AXMP	—	±0.68	±2.04		
			S-80959AXMP	—	±0.69	±2.07		
			S-80960AXMP	—	±0.71	±2.13		

■ Test Circuits



* R is unnecessary for CMOS output products.



* R is unnecessary for CMOS output products.

Figure 4

■ Technical Terms

1. Detection voltage ($-V_{DET}$)

The detection voltage $-V_{DET}$ is the voltage at which the output switches to low. This detection voltage varies slightly among products of the same type. The variation of voltages between the specified minimum [$(-V_{DET})$min.] and maximum [$(-V_{DET})$max.] values is called the detection voltage range (See Figure 5).

Example : For the S-80915AN, detection voltage lies in the range of $1.470 \leq (-V_{DET}) \leq 1.530$.
This means that $-V_{DET}$ is 1.470 in a product while $-V_{DET}$ is 1.530 in another of the same S-80915AN.

2. Release voltage ($+V_{DET}$)

The release voltage $+V_{DET}$ is the voltage at which the output returns (is "released") to high. This release voltage varies slightly among products of the same type. The variation of voltages between the specified minimum [$(+V_{DET})$min.] and maximum [$(+V_{DET})$max.] values is called the release voltage range (See Figure 6).

Example : For the S-80915AN, the release voltage lies in the range of $1.514 \leq (+V_{DET}) \leq 1.652$. This means that $+V_{DET}$ is 1.514 in a product while $+V_{DET}$ is 1.652 in another of the same S-80915AN.

Remark: Although the detection voltage and release voltage overlap in the range of 1.514 V to 1.530 V, $+V_{DET}$ will always be larger than $-V_{DET}$.

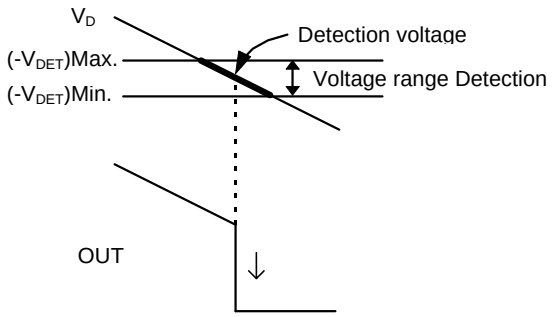


Figure 5

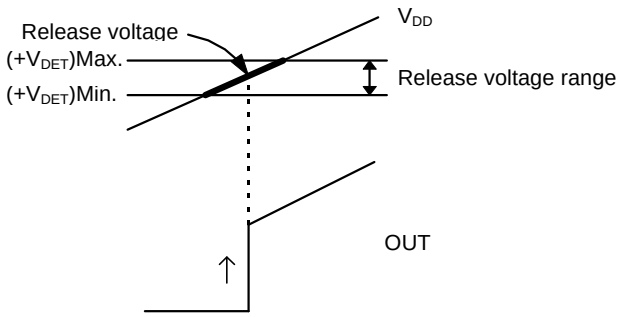


Figure 6 (C_D=0F)

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (B-A=V_{HYS} in Figure 11). By giving a device hysteresis, trouble such as noise at the input is avoided.

4. Delay time (td)

The delay time is a time that the input voltage to V_{DD} terminal exceeds the release voltage ($+V_{DET}$) and then the output of the OUT terminal inverts. The delay time can be changed by the additional external capacitor C_D.

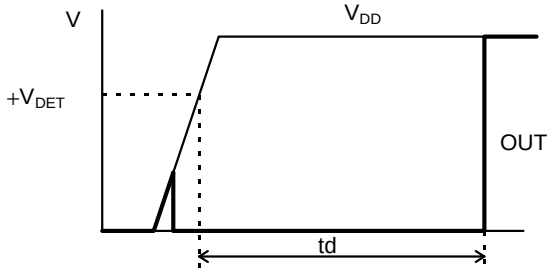


Figure 7

5. Through-type current

Through-type current refers to the current which flows instantaneously at the time of detection and release of a voltage detector. Through-type current is large in CMOS output devices, and also flows to some extent in Nch open-drain output devices.

6. Oscillation

In applications where a resistor is connected to the voltage detector input (Figure 8), in the CMOS active low products for example, the through-type current generated when the output goes from low to high (release) causes a voltage drop equal to [through-type current] × [input resistance] across the resistor. When the resultant input voltage drops below the detection voltage $-V_{DET}$, the output voltage returns to its low level. In this state, the through-type current and its resultant voltage drop have disappeared, and the output goes back from low to high. A through-type current is again generated, a voltage drop appears, and the process repeats. This unstable condition is referred to as oscillation.

・ Misimplementation with input voltage divider

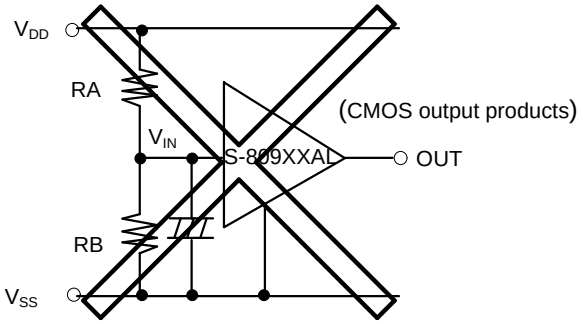
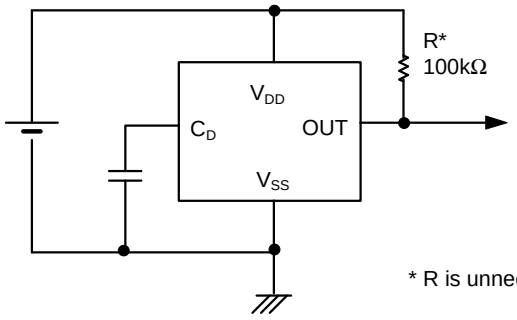


Figure 8

■ Standard Circuit



* R is unnecessary for CMOS output products.

Figure 9

Connect directly the C_D capacitor for delay between C_D and V_{SS} terminals.

■ Operation

1. Basic operation : CMOS active low output

(1) When power supply voltage V_{DD} is greater than the release voltage $+V_{DET}$, the Nch transistor is OFF and the Pch transistor ON, causing V_{DD} (high) to appear at the output. With the Nch transistor N1 of Figure 10 OFF, the comparator input voltage is $(RB+RC)/(RA+RB+RC \times V_{DD}$.

(2) When power supply voltage V_{DD} goes below $+V_{DET}$, the output maintains the power supply voltage level, as long as V_{DD} remains above the detection voltage $-V_{DET}$. When V_{DD} does fall below $-V_{DET}$ (A in Figure 11), the Nch transistor goes ON, the Pch transistor goes OFF, and V_{SS} appears at the output. With the Nch transistor N 1 of Figure 10 ON, the comparator input voltage is $RB/(RA+RB) \times V_{DD}$.

(3) When V_{DD} falls below the minimum operating voltage, the output becomes undefined. However, output will revert to V_{DD} if a pull-up has been employed.

(4) V_{SS} will again be output when V_{DD} rises above the minimum operating voltage. V_{SS} will continue to be output even when V_{DD} surpasses $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.

(5) When V_{DD} rises above $+V_{DET}$ (B in Figure 11), the Nch transistor goes OFF, the Pch transistor goes ON, and V_{DD} appears at the output. Then V_{DD} at the OUT terminal appears with delay time(td) due to delay circuit.

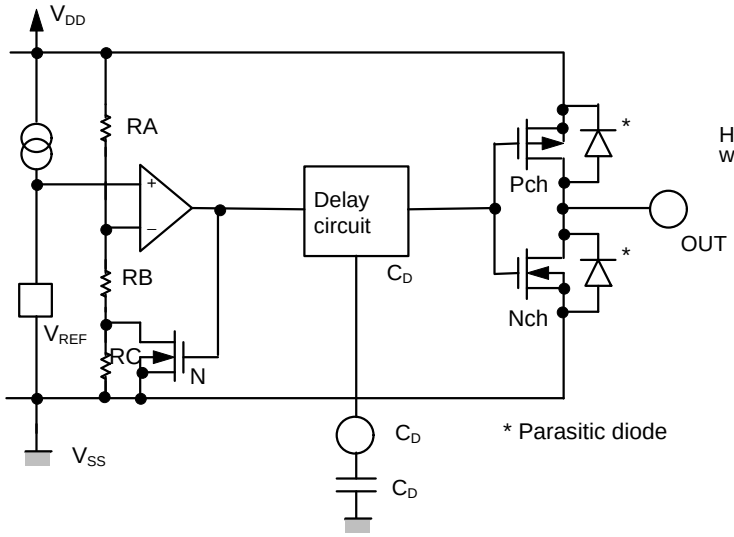


Figure 10

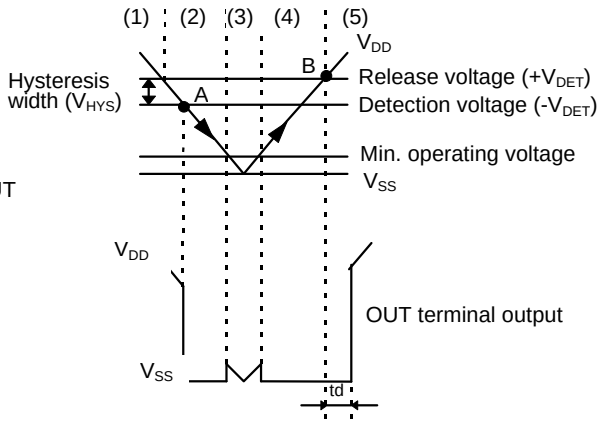


Figure 11

2. Delay circuit

The delay circuit outputs the signal delayed from the release voltage ($+V_{DET}$) point of the power voltage V_{DD} rising. The output signal is not delayed when the V_{DD} goes down the detection voltage ($-V_{DET}$) or less. (See Figure 11). The delay time(td) is determined by the time constant of the built-in constant current (approx. 100nA in the case of products with detection voltage of 1.5V or more, approx. 570nA in the case of products with detection voltage of 1.4V or less) and the attached external capacitor (C_D), and calculated from the following formula.

td (ms) = Delay factor $\times$ C_D (nF)

Delay factor: (25°C)

Products with detection voltage of 1.4V or less		: Min.0.57, Typ.0.77, Max.0.96
Products with detection voltage of 1.5V or more	Nch open-drain outputs	: Min.4.3, Typ.5.7, Max.7.2
	CMOS outputs	: Min.3.8, Typ.5.1, Max.6.4

[Cautions]

- The open of C_D terminal may cause double pulses shown in Figure 12 at release.
  If the double pulses cause a trouble, attach 10pF or larger capacitor to the C_D terminal.
  Do not apply the voltage to the C_D terminal.

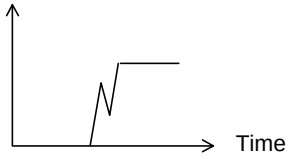


Figure 12

- Layout the print circuit board not to apply or flow out the current to/from the CD terminal. Doing not so may cause inaccurate delay time..
- Use an external capacitor, CD of which leakage current can be ignored for the built-in constant-current value. A leakage current may cause an error of delay time. Also, a leakage current over the built-in constant-current causes unrelease status.

3. Other characteristics

(1) Temperature characteristic of detection voltage

The temperature characteristics of the detection voltage are expressed by the oblique line parts in Figure 12.

S-80915AXMP:

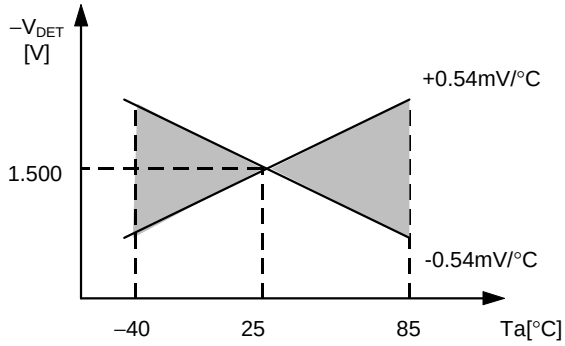


Figure 13

(2) Temperature characteristics of release voltage

The temperature factor $\left(\frac{\Delta+V_{DET}}{\Delta Ta}\right)$ of the release voltage is calculated by the temperature factor of the detection voltage as follows:

$$\frac{\Delta+V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta-V_{DET}}{\Delta Ta}$$

The temperature factor of the release voltage has a same sign characteristics as the temperature factor of the detection voltage.

(3) Temperature characteristics of hysteresis voltage

The temperature characteristics of hysteresis voltage $\left(\frac{\Delta+V_{DE}}{\Delta Ta} - \frac{\Delta-V_{DET}}{\Delta Ta}\right)$ is calculated as follows:

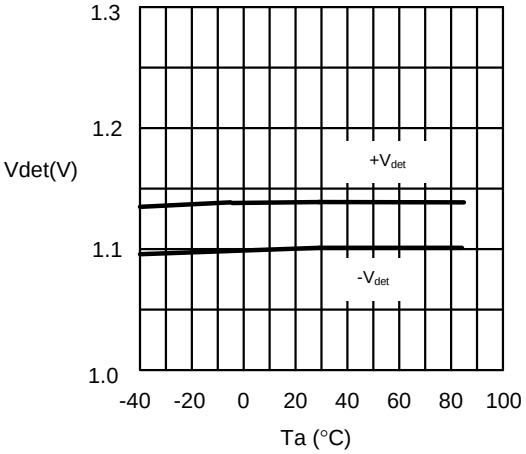
$$\frac{\Delta+V_{DET}}{\Delta Ta} - \frac{\Delta-V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta-V_{DET}}{\Delta Ta}$$

Samples of each temperature characteristics for (1) to (3) are shown in page 14 to page 15.

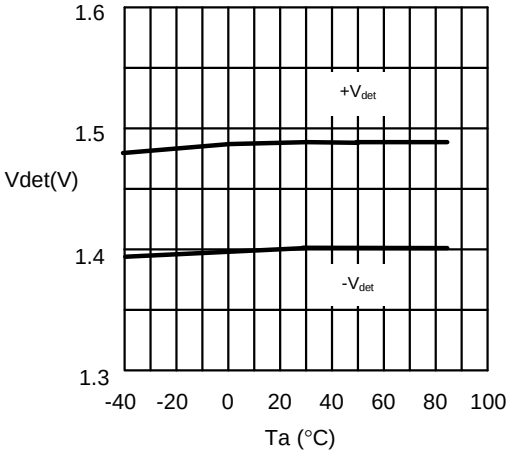
■ Characteristics (typical characteristics)

(1) Detection voltage (V_{DET}) - Temperature (Ta)

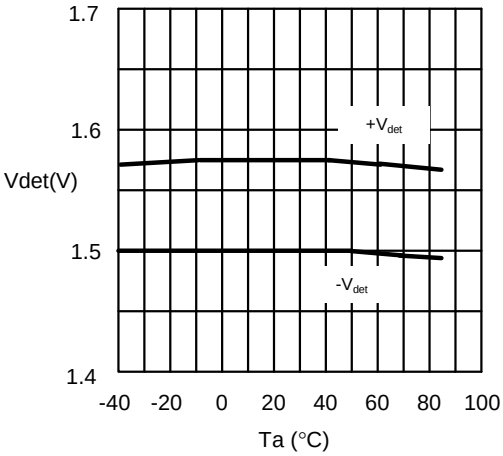
(a) S-80911AN



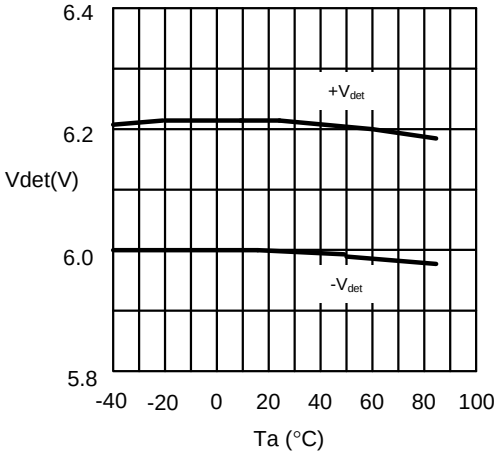
(b) S-80914AN



(c) S-80915AN

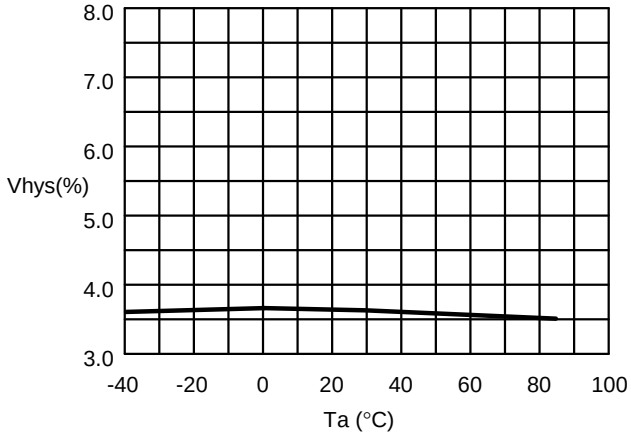


(d) S-80960AN

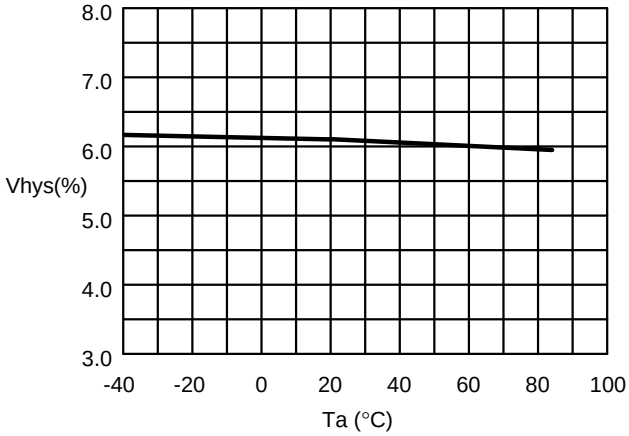


(2) Hysteresis voltage width (Vhys) - Temperature (Ta)

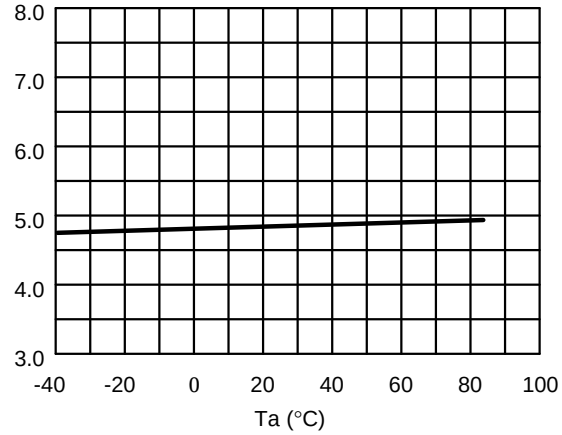
(a) S-80911AN



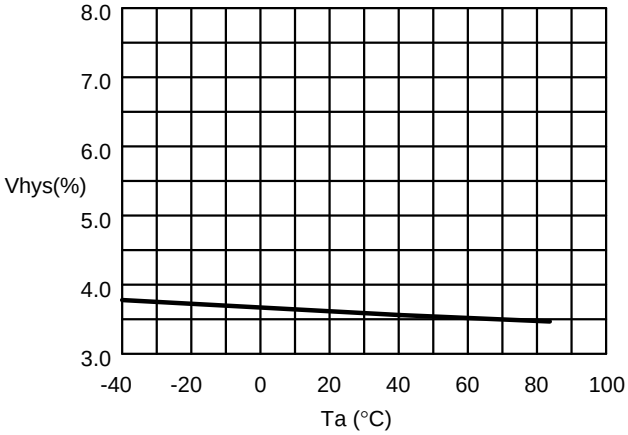
(b) S-80914AN



(c) S-80915AN

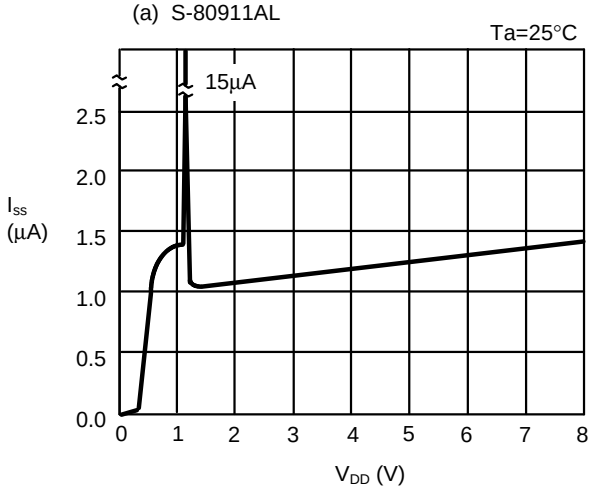


(d) S-80960AN

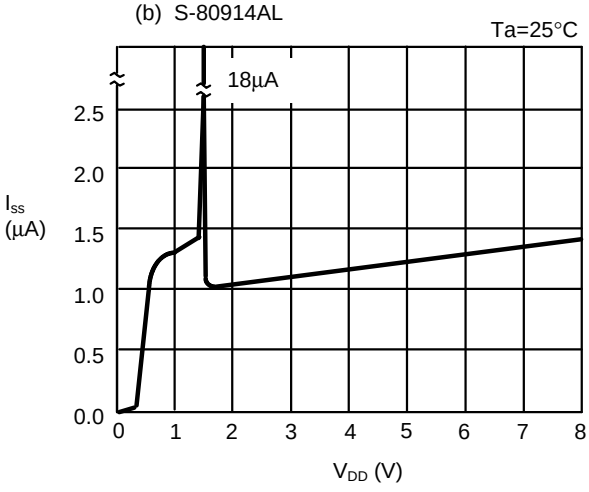


(3) Current consumption (I_{SS}) - Input voltage (V_{DD})

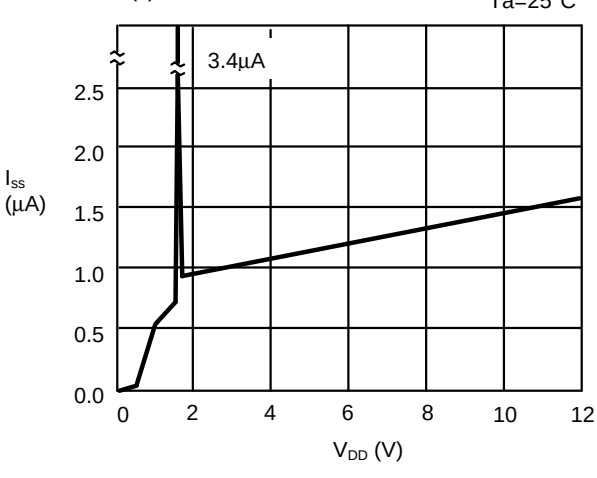
(a) S-80911AL



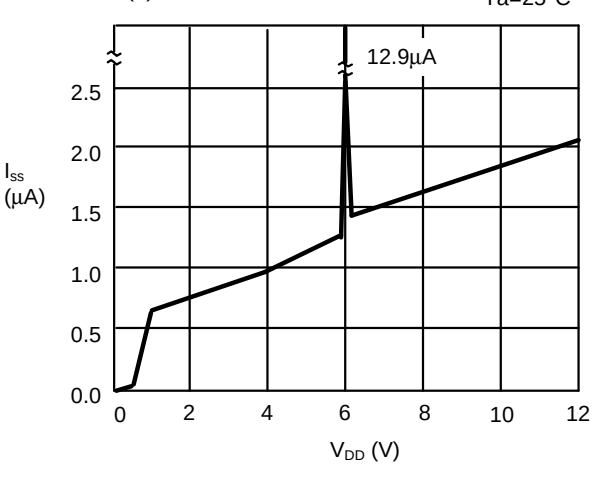
(b) S-80914AL



(c) S-80915AL

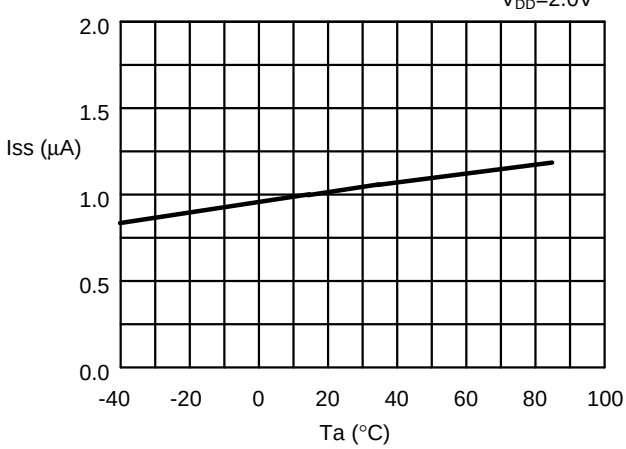


(d) S-80960AL

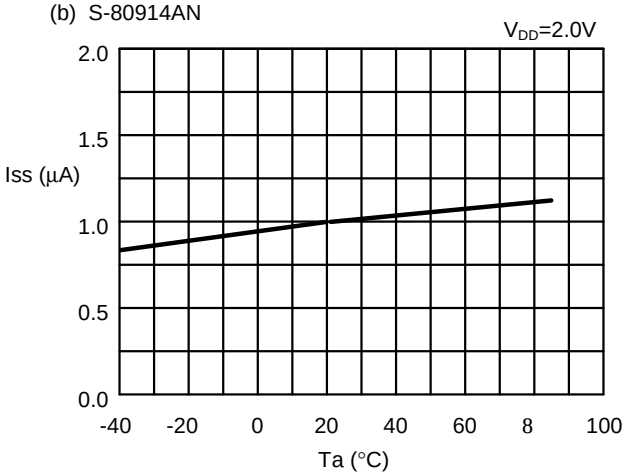


(4) Current consumption (I_{SS}) - Temperature (Ta)

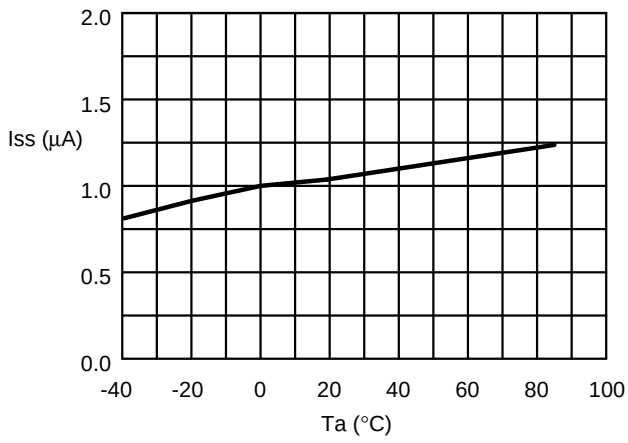
(a) S-80911AN



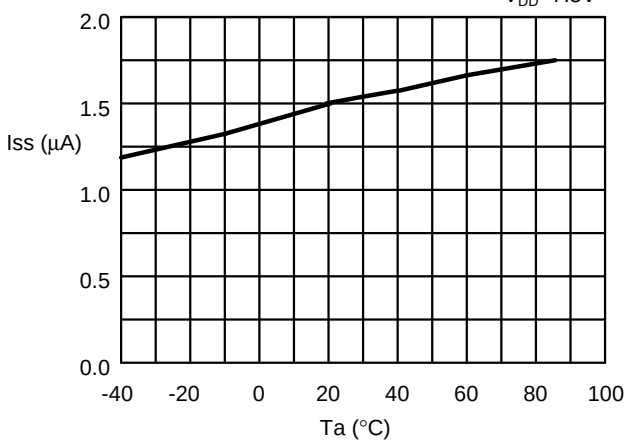
(b) S-80914AN



(c) S-80915AN

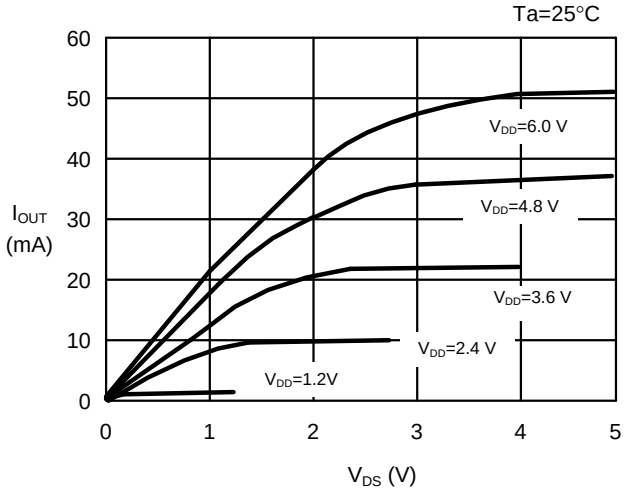


(d) S-80960AN



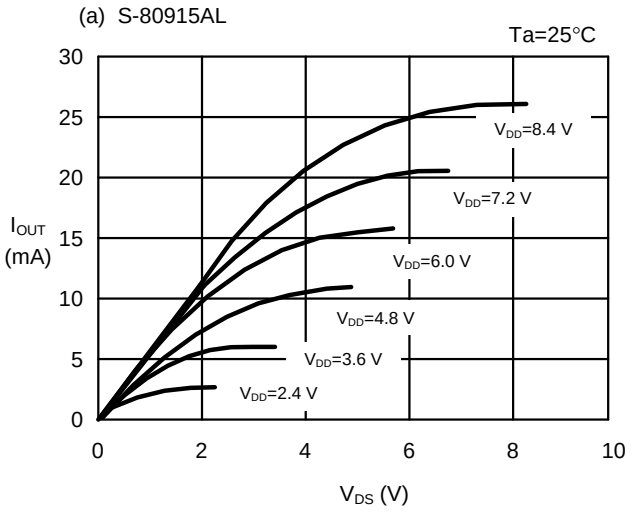
(5) Nch transistor output current (I_{OUT}) - V_{DS}

(a) S-80960AL



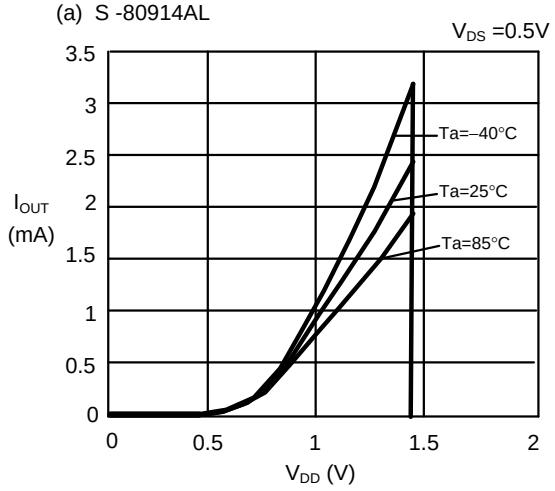
(6) Pch transistor output current (I_{OUT}) - V_{DS}

(a) S-80915AL

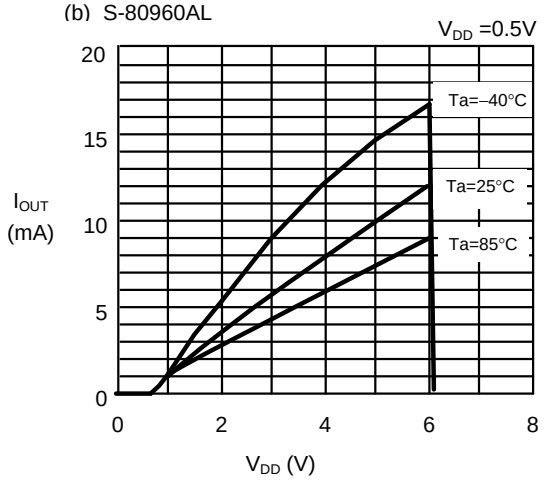


(7) Nch transistor output current (I_{OUT}) - Input voltage(V_{DD})

(a) S -80914AL

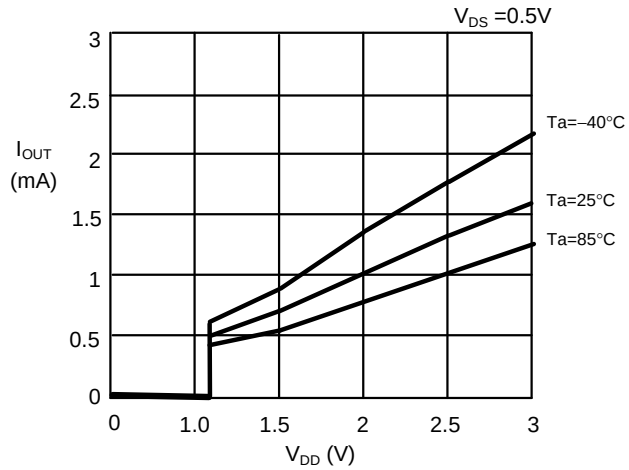


(b) S-80960AL

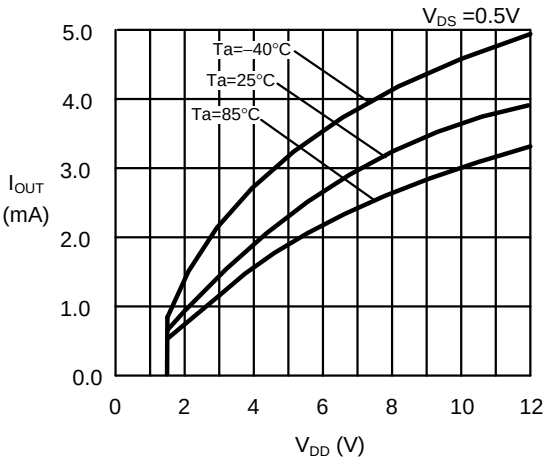


(8) Pch transistor output current(IOUT) - Input voltage(VDD)

(a) S-80911AL

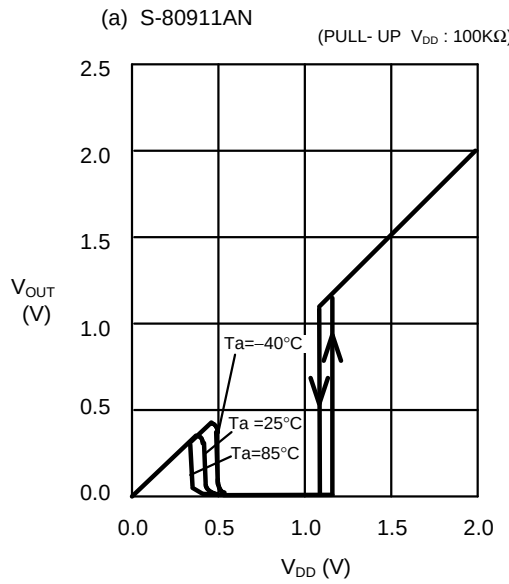


(b) S-80915AL

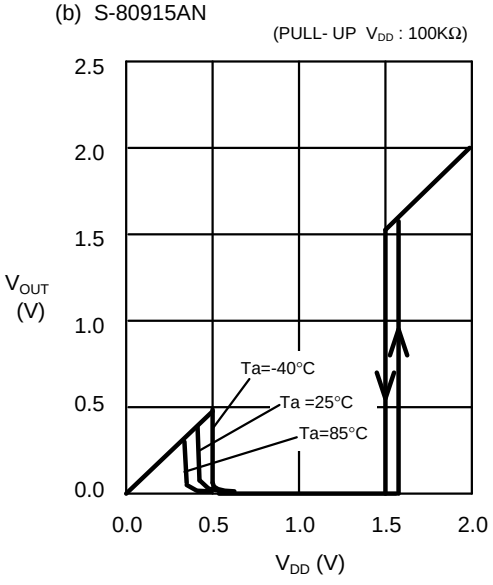


(9) Minimum operating voltage

(a) S-80911AN

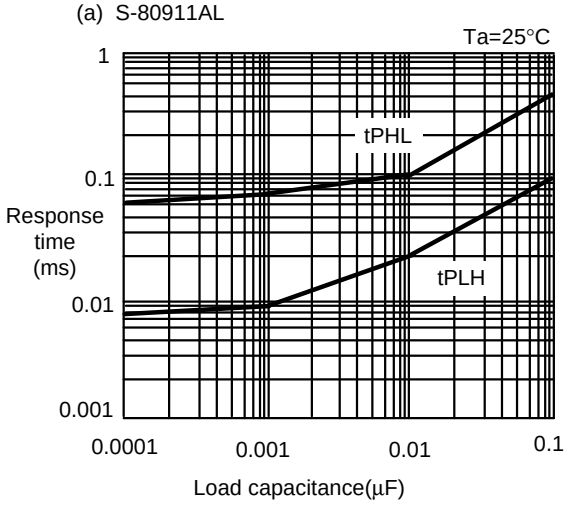


(b) S-80915AN



(10) Dynamic response (C_D : Open)

(a) S-80911AL



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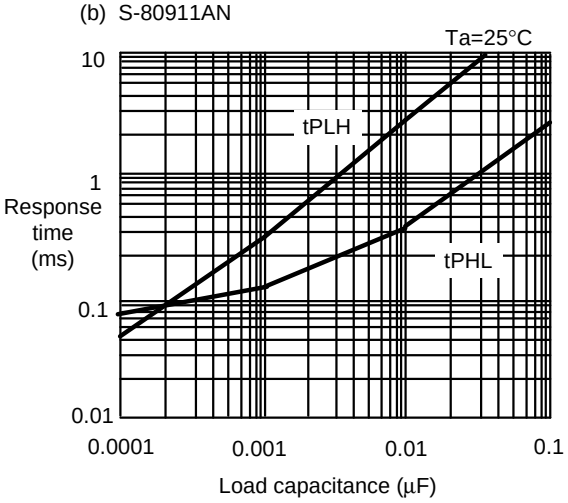
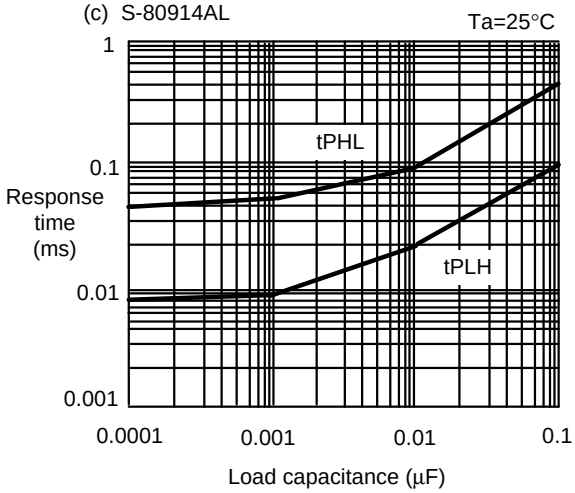
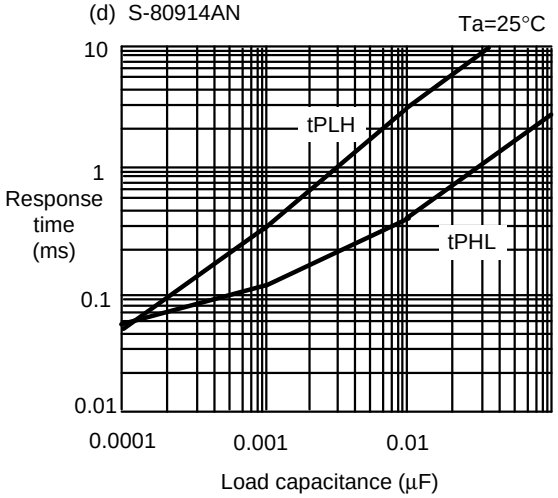


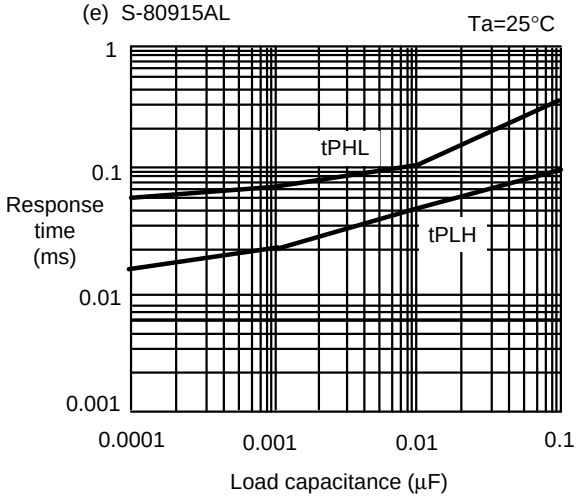
(c) S-80914AL



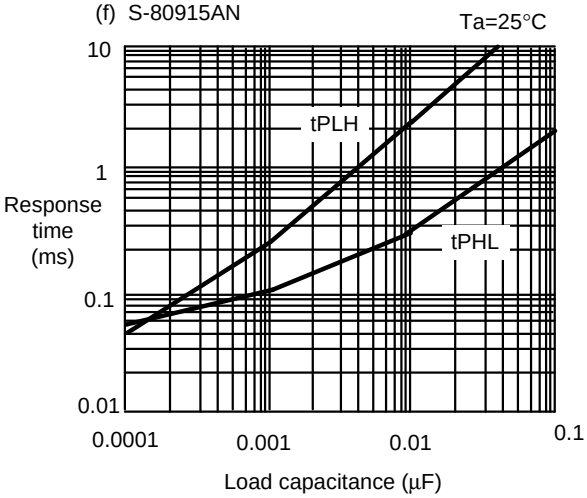
(d) S-80914AN



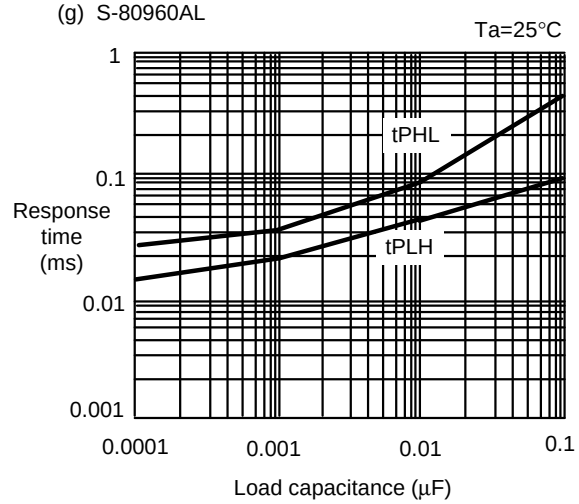
(e) S-80915AL



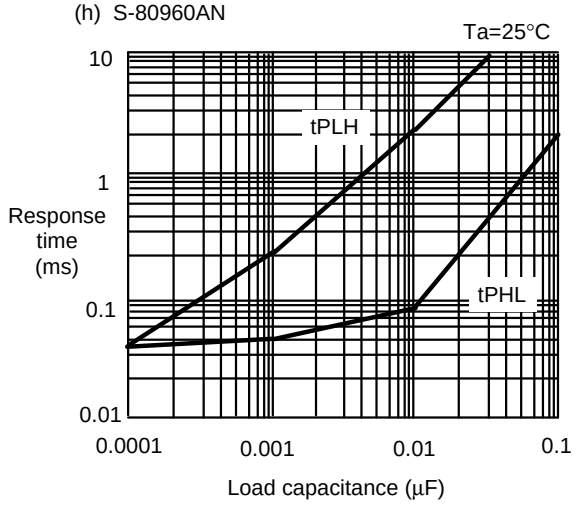
(f) S-80915AN

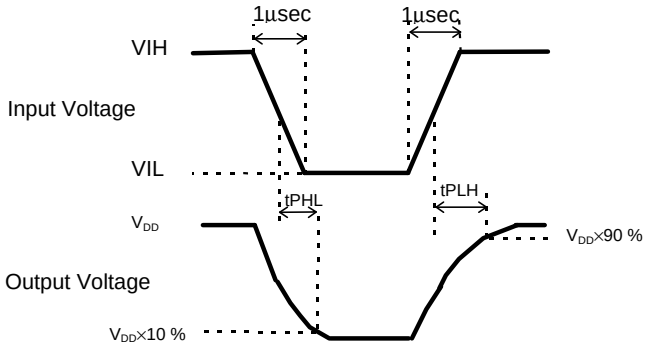


(g) S-80960AL



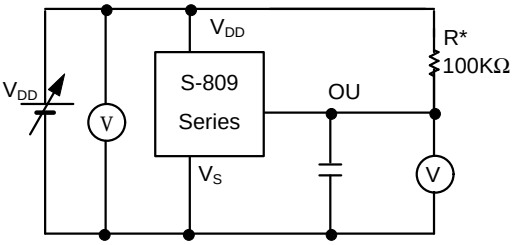
(h) S-80960AN





(a)to(d) : VIH=6V, VIL=0.80V
(e)to(h) : VIH=10V, VIL=0.95V

Figure 14 Measuring conditions of response time

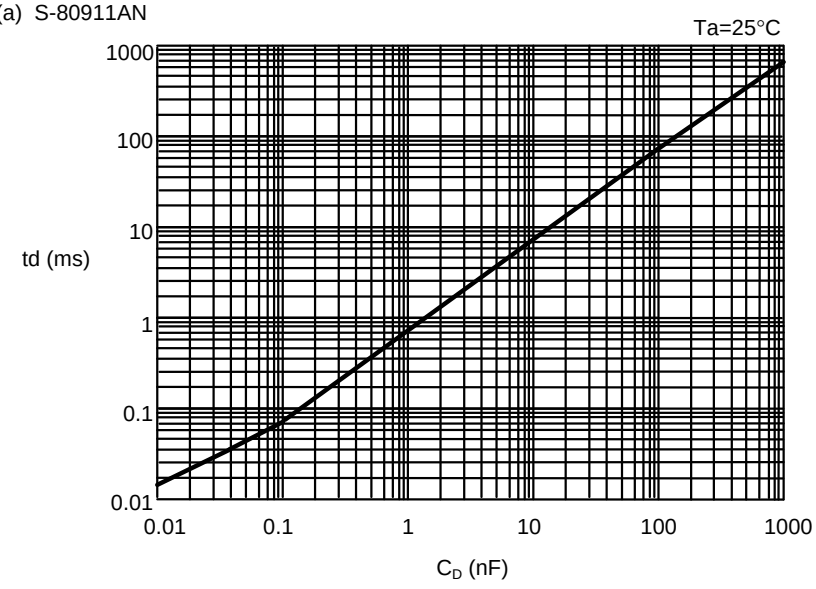


*'R' is not needed for CMOS output products.

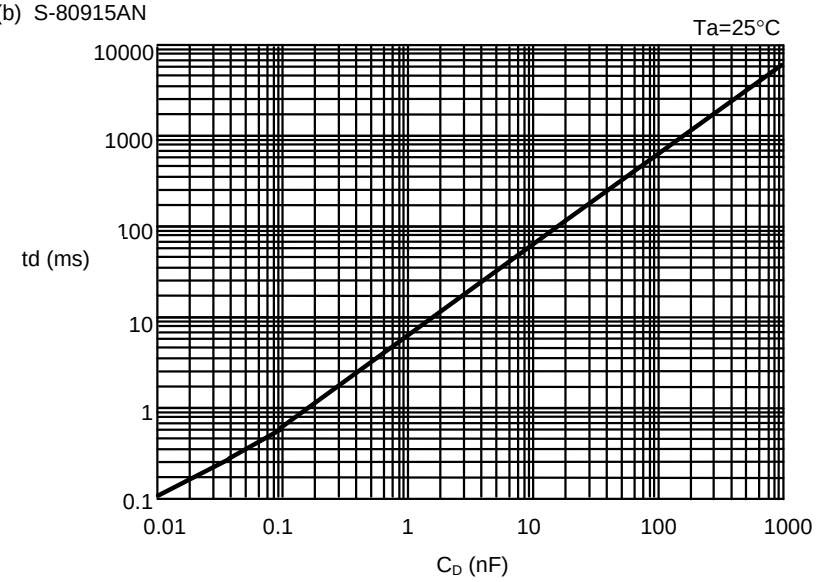
Figure 15 Measuring circuit of response time

(11) Delay time (td) - External capacitor(C_D)

(a) S-80911AN

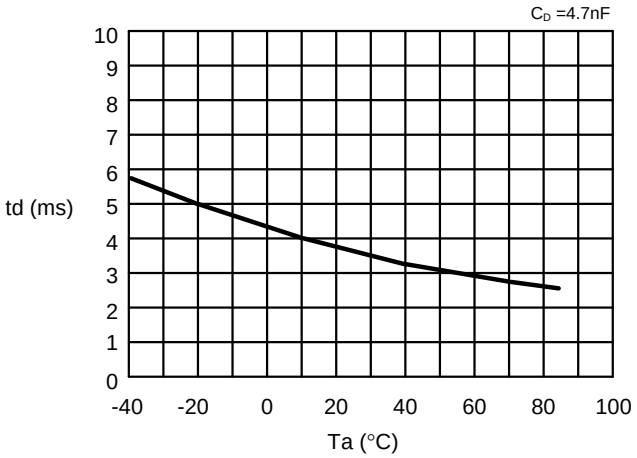


(b) S-80915AN

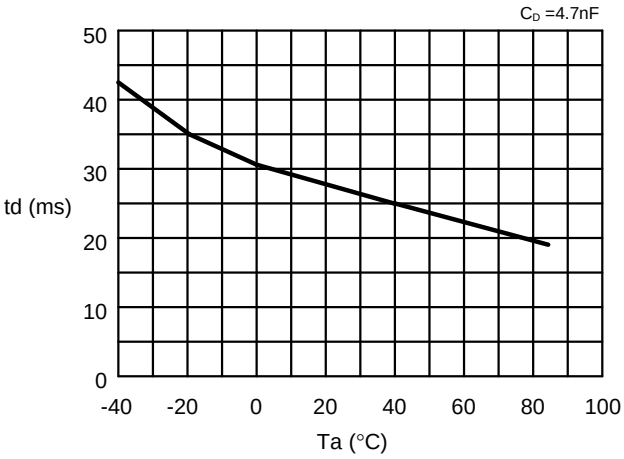


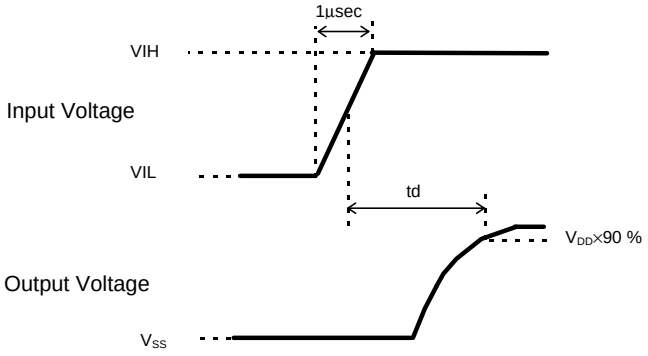
(12) Delay time (tpd) - Temperature (Ta)

(a) S-80911AN



(b) S-80915AN





(a) : VIH=6V, VIL=0.80V
(b) : VIH=10V, VIL=0.95V

Figure 16 Measuring conditions of delay time

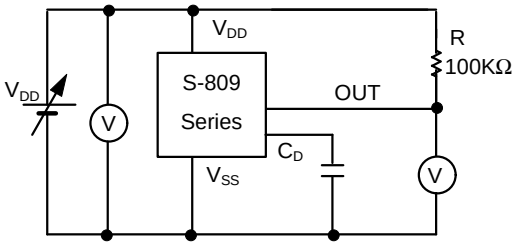


Figure 17 Measuring circuit of delay time

■ Application Circuit Examples

1. Microcomputer reset circuits

With the S-809 Series which has a low operating voltage, a high-precision detection voltage and hysteresis characteristic, the reset circuits shown in Figures 18 to 19 can be easily constructed.

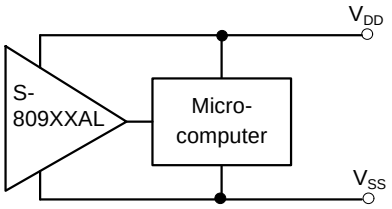
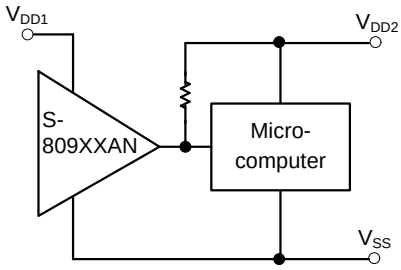


Figure 18

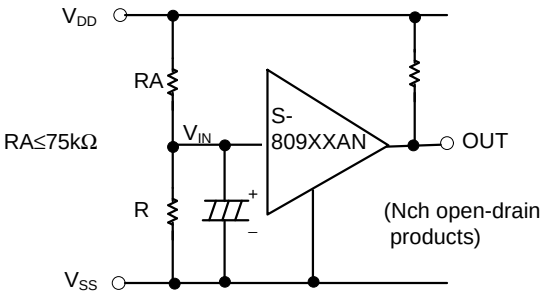


(Nch open-drain output products only)

Figure 19

2. Change of detection voltege

In Nch open-drain output products of the S-809 Series, detection voltage can be changed using resistance dividers or diodes as shown in Figures 20 and 21. In Figure 20, hysteresis width is also changed.

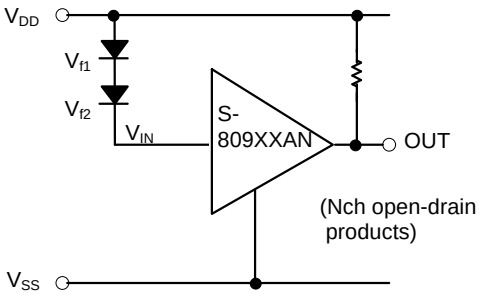


$$\text{Detection voltage} = \frac{RA+RB}{RB} \cdot -V_{DET}$$

$$\text{Hysteresis width} = \frac{RA+RB}{RB} \cdot V_{HYS}$$

Note1: If RA and RB are large, the hysteresis width may be larger than the value given by the formula above due to through type current (which flows slightly in Nch open-drain circuit).
Note2: RA should be 75kΩor less to prevent oscilation.

Figure 20



Detection voltage $=V_{f1}+V_{f2}+(-V_{DET})$

Figure 21

■ Notes

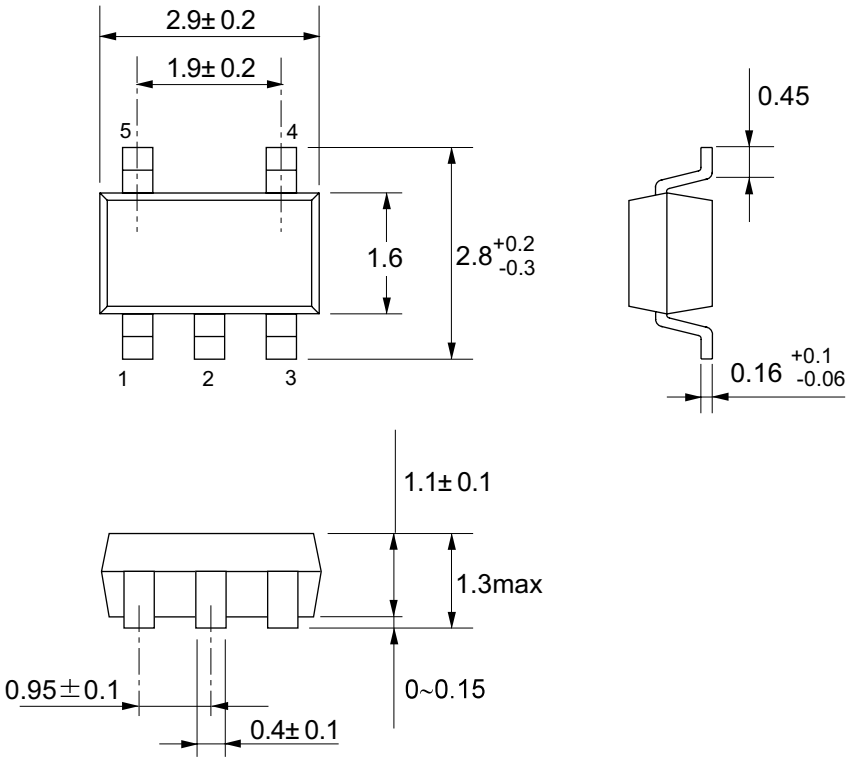
- In CMOS output products of the S-809 Series, through type current flows when the device is detecting or releasing. If a high impedance is connected to the input, oscillation may be caused due to the fall of the voltage by the through type current when lowering the voltage during releasing.
- When designing for mass production using an application circuit described herein, take the product deviation and temperature characteristic into consideration.
- Seiko Instruments Inc. shall not bear any responsibility for the patents on the circuits described herein.

■ SOT-23-5

MP005-A 991105

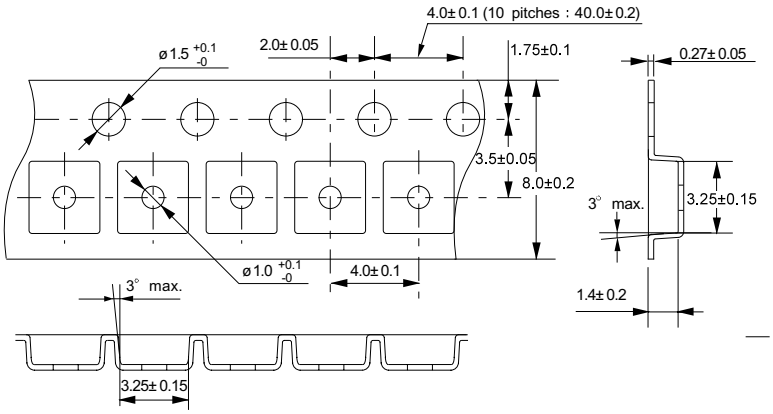
Unit : mm

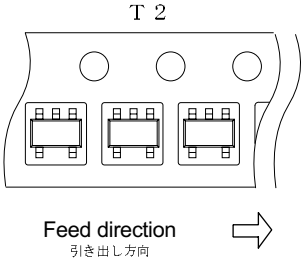
● Dimensions 外形図



No. : MP005-A-P-SD-1.1

● Taping Specifications テーピング図

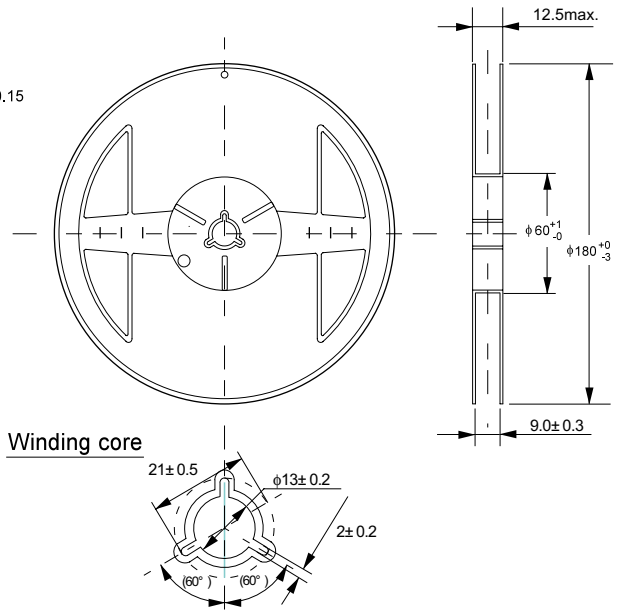




No. : MP005-A-C-SD-1.0

● Reel Specifications リール図

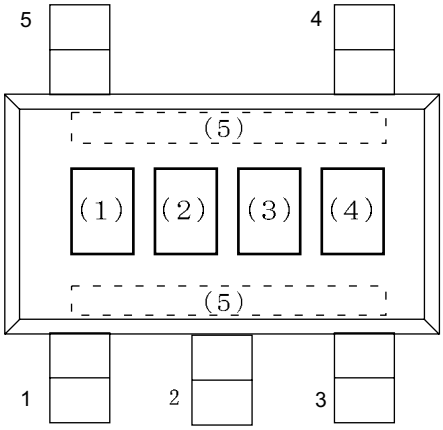
3000 pcs./reel



No. : MP005-A-R-SD-1.0

■Markings

● SOT-23-5



(1) to (3) : Product name (abbreviation)

(4) : Month of assembly

(5) : Dot on one side (Year and week of assembly)

No.：MP005－A－M－S1－1．0

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