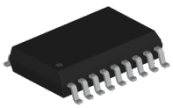
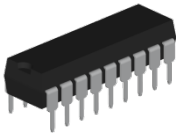
8-Channel Darlington Current Driver TD62783A

FEATURES

- 8 Darlington Arrays per Package
- Minus 500 mA (Source) Output Current (Single Output)
- Output voltage 50V
- Output Clamp Diodes
- Input Compatible with Various Types of Logic
- Relay-Driver Applications
- Input pins placed opposite to output pins to simplify layout



SOP-18



DIP-18

APPLICATION

- Relay Drivers
- Stepper and DC Brushed Motor Drivers
- Lamp Drivers
- Display Drivers
- Line Drivers
- Logic Buffers

DESCRIPTION

The TD62783A is monolithic high-voltage, high-current Darlington transistor arrays. Each consists of eight NPN Darlington pairs that feature high-voltage outputs with common-anode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is minus 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

ORDERING INFORMATION

Device	Package
TD62783AD	SOP-18
TD62783AN	DIP-18

ABSOLUTE MAXIMUM RATINGS (Note 1,2)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	V_{CC}	-	50	V
Input Voltage	V_{IN}	-	15	V
Output Current	I_{OUT}	-	−500	mA
Clamp Diode Reverse Voltage	V_R	-	50	V
Clamp Diode Forward Current	I_F	-	500	mA
Maximum Junction Temperature	T_J	-	150	°C

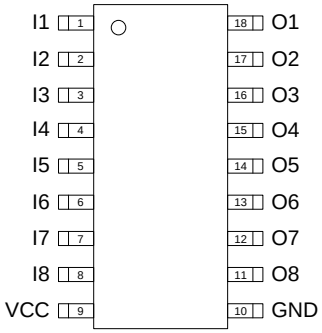
RECOMMENDED OPERATIONG CONDITIONS (Note 2)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	V_{CC}	-	50	V
Output Current	I_{OUT}	-	−350	mA
Clamp Diode Reverse Voltage	V_R	-	50	V
Clamp Diode Forward Current	I_F	-	400	mA
Junction Temperature	T_J	−40	125	°C
Operating Free-Air Temperature Range	T_A	−40	85	°C

ORDERING INFORMATION

Package	Order No.	Description	Package Marking	Status
SOP-18	TD62783AD	8-Channel Darlington Current Driver	TD62783A	Active
DIP-18	TD62783AN	8-Channel Darlington Current Driver	TD62783A	Contact Us

PIN CONFIGURATION

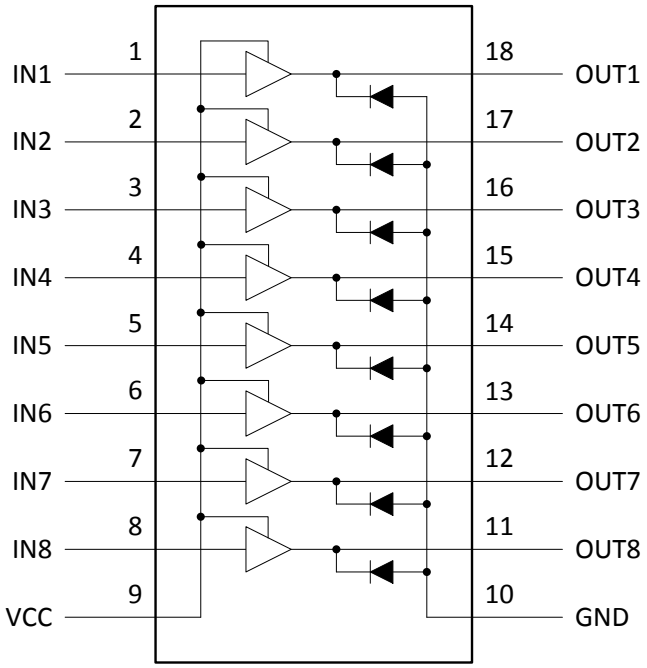


SOP-18 / DIP-18

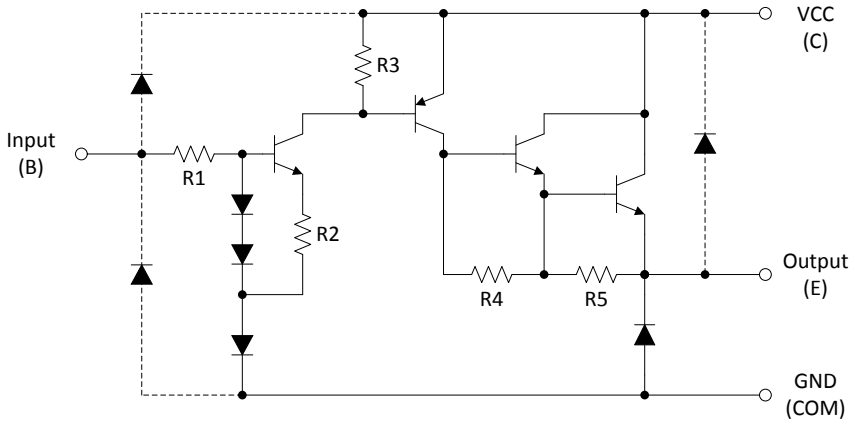
PIN DESCRIPTION

Pin No.		Pin Name	Pin Function
SOP-18	DIP-18		
1	1	I1	Channel 1 through 8 Darlington Base Input
2	2	I2	
3	3	I3	
4	4	I4	
5	5	I5	
6	6	I6	
7	7	I7	
8	8	I8	
9	9	VCC	Power Supply
10	10	GND	Ground
11	11	O8	Channel 1 through 8 Darlington Emitter Output
12	12	O7	
13	13	O6	
14	14	O5	
15	15	O4	
16	16	O3	
17	17	O2	
18	18	O1	

PIN CONNECTION DIAGRAM



BLOCK DIAGRAM



R1: 10 kΩ
R2: 2.6 kΩ
R3: 20 kΩ
R4: 10 kΩ
R5: 5.0 kΩ

ELECTRICAL CHARACTERISTICS (Note 3)

Limits in standard typeface are for T_A=25°C, unless otherwise specified.

PARAMETER	SYMBOL	TEST FIGURE	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leakage Current	I_{CEX}	Fig. 1	V_{CC} = 50V, V_{IN} = 0.4V	-	-	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	Fig. 2	V_{IN} = 2V, I_{OUT} = −100mA	-	-	1.8	V
			V_{IN} = 2V, I_{OUT} = −225mA	-	-	1.9	
			V_{IN} = 2V, I_{OUT} = −350mA	-	-	2.0	
Input Current	$I_{IN(ON)}$	Fig. 3	V_{IN} = 2.4V	-	-	52	μA
			V_{IN} = 3.85V	-	-	260	
Input Voltage at ON state	$V_{IN(ON)}$	Fig. 4	V_{CE} = 2.0V, I_{OUT} = −350mA	-	-	2.0	V
Input Voltage at OFF state	$V_{IN(OFF)}$	Fig. 4	I_{OUT} = −500μA	0.8	-	-	V
Supply Current	$I_{CC(ON)}$	Fig. 3	V_{CC} = 50V, V_{IN} = 2V	-	-	2.5	mA
Clamp Diode Reverse Current	I_R	Fig. 5	V_R = 50V	-	-	50	μA
Clamp Diode Forward Voltage	V_F	Fig. 6	I_F = 350mA	-	-	2.0	V
Turn-On Propagation Delay Time	t_{ON}	Fig. 7	V_{CC} = 50V, R_L = 125, C_L = 15pF	-	0.15	-	μs
Turn-Off Propagation Delay Time	t_{OFF}	Fig. 7	V_{CC} = 50V, R_L = 125, C_L = 15pF	-	3.0	-	

Note 1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2. All voltage values are with respect to the GND, unless otherwise noted.

Note 3. The device is not guaranteed to function outside its operating ratings.

PARAMETER MEASUREMENT INFORMATION

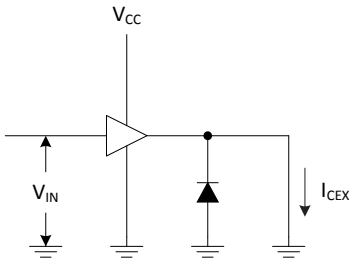


Fig. 1. I_{CEX} Test Circuit

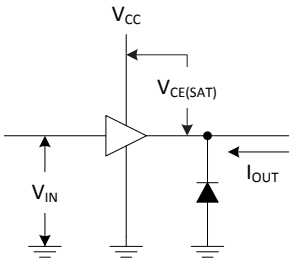


Fig. 2. $V_{CE(SAT)}$ Test Circuit

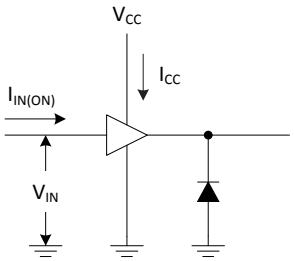


Fig. 3. $I_{IN(ON)}$, I_{CC} Test Circuit

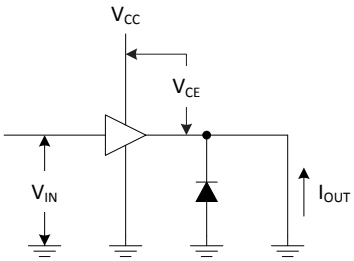


Fig. 4. $V_{IN(ON)}$, $V_{IN(OFF)}$ Test Circuit

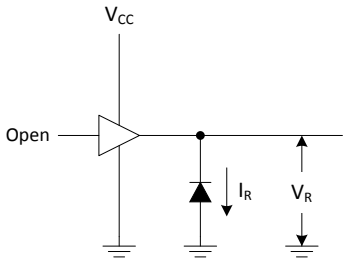


Fig. 5. I_R Test Circuit

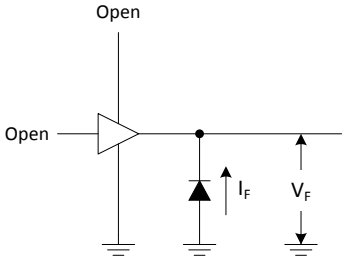
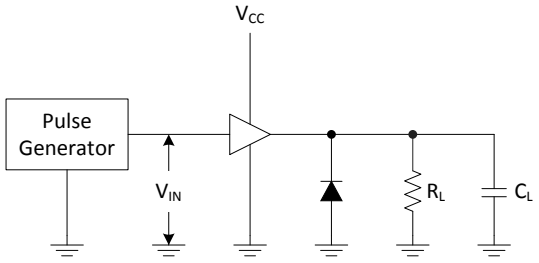
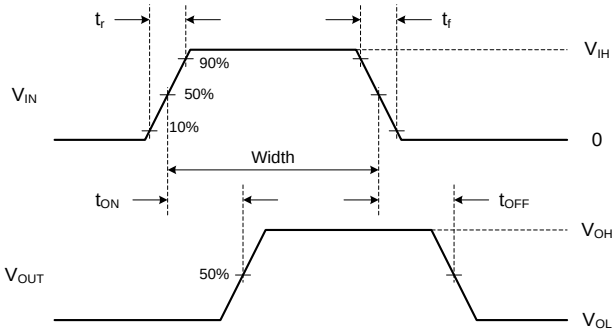


Fig. 6. V_F Test Circuit



* C_L includes probe and jig capacitance.

Fig. 7. t_{ON}, t_{OFF} Test Circuit



* Pulse Width 50μs, Duty Cycle 10%, $t_r \le 5ns$, $t_f \le 10ns$

Fig. 8. Propagation Delay Time Waveform

TYPICAL OPERATING CHARACTERISTICS

T.B.D.

REVISION NOTICE

The description in this datasheet is subject to change without any notice to describe its electrical characteristics properly.