電界強度計キット

小型ハンディ
測定帯域：10MHz標準（DC～300MHz）

《小型》ハンディ 電界強度計キット ver.2

測定帯域：１０MHz標準（１MHz～３００MHz）
感知限界：min１００kHz,　　max１GHz
感知強度：３０dBμV（−７７dBm）～１２５dBμV（＋１８dBm）

■キット概要■
機械式アナログメーター表示，
７段ロッドアンテナ（１０cm～８０cm）付，
シールドケース付，　ＨＩ，ＬＯレンジ選択（切替）可
電源：ＤＣ９Ｖ１０mA（００６Ｐ９Ｖ電池）

■部品■

□半導体

ＡＤ８３０７　スペシャルＩＣ		１個
ＣＡ３１４０　オペアンプ		１個
Ｓ８１３５０　低ドロップ５Ｖレギュレータ		１個

□抵抗

１０Ω	1/4W	茶黒黒金（銀）		２個
５１Ω	1/4W	緑茶黒金		１個
５．６ｋΩ	1/4W	緑青赤金		１個
※２０ｋΩ	1/4W	赤黒橙金	GBW-670（50μA）用	１個
※２２ｋΩ	1/4W	赤赤橙金	GBW-520（50μA）用	１個
※１１ｋΩ	1/4W	茶茶橙金	DE-550（100μA）用	１個

□コンデンサ

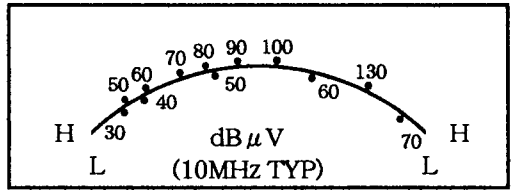
０．０１μＦ	（103）セラミック	２個
０．１μＦ	（104）セラミック	４個
１０～１００μＦ	電解コンデンサ	１個

□その他
基板，シールドケース，アンテナ，変換コネクタ，メーター，
００６Pスナップ，ＩＣソケット２個
御用意ください　➡　配線用リード線（ビニル被覆線など）
※［　付属メーターのタイプによって選択して取り付け　］

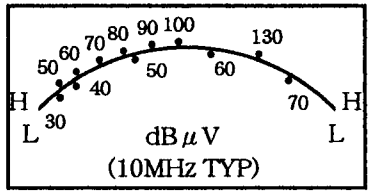
《メーター対応表》

付属メーターのタイプ　　貼付用校正済み目盛り
➡※選択する抵抗

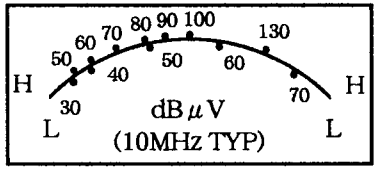
GBW-670（50μA）
➡※２０kΩ



GBW-520（50μA）
➡※２２kΩ



DE-550（100μA）
➡※１１kΩ

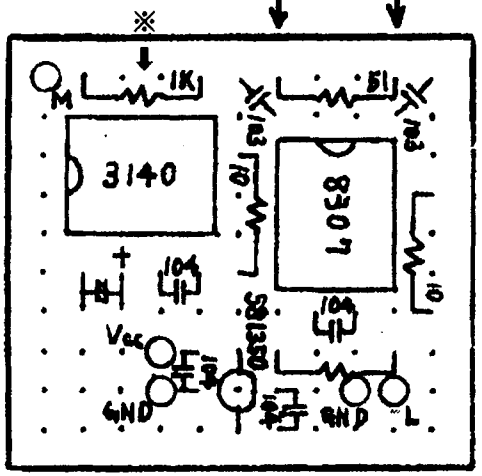


■キットに関する御質問について■
御面倒ですが、往復ハガキor返信用切手同封の封書に於いてのみ、御受けできます。申し訳ありませんが、電話回線混雑の為、電話およびＦＡＸでは、御返答できません。

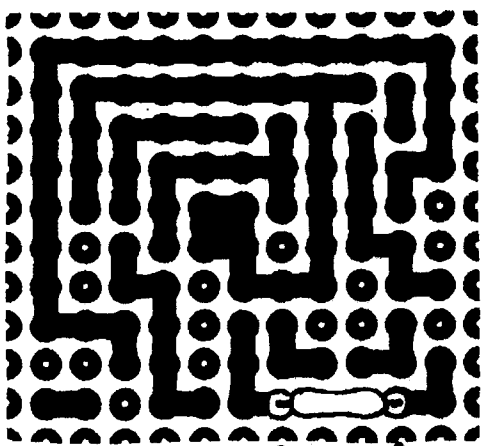
〒158-0095　東京都世田谷区瀬田5-35-6
（有）秋月電子通商　キット御質問受付係

付属メータのタイプによって
取り付け抵抗を選択

アース　アンテナ



←基板おもて



←基板うら

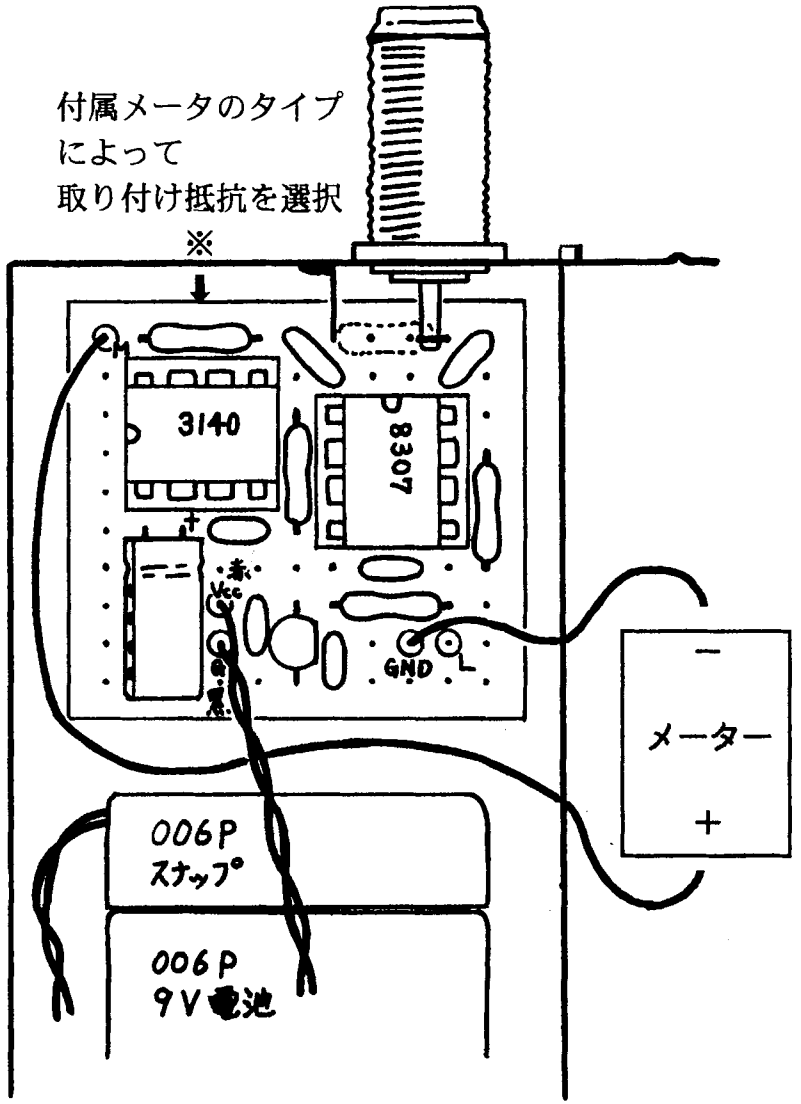
51Ω

アース　アンテナ

配線、部品
取り付け➡

《実体図》

付属メータのタイプ
によって
取り付け抵抗を選択
※



※工作は《**実体図**》を参照しながら行って下さい。

■工作１／３■基板の切断----------

シールドケースに入れる為には、デザインナイフや模型用工作ノコなどで、基板の切断をします。この作業は、作業性を考慮して、部品取り付け作業より以前に行うのが適切です。基板の孔列上に印刷された線に沿って切断します。

ナイフで切断する場合には、基板の裏表両面から何回も筋目を入れ、最後に「パキッ」と折ります。この際、筋入れが甘かったり、折るべき所から遠い所を持って迂闊に力を入れると、思わぬ所で折れてしまうので、御注意ください。

どちらの場合も、切断面は、できれば、ヤスリなどを用いて、きれいに仕上げましょう。特に、ランドかす等の金屑は、ショートトラブルを起こすので、要注意です。

■工作２／３■基板の組立----------

ここで、注意して頂きたいのは、基板印刷の【５１】に取り付ける抵抗【５１Ω】のみは、基板の裏面から、足を切断せずに取り付けることです。足は、工作３／３で、接続に使用します。

そして、基板印刷の【１Ｋ】に取り付ける抵抗【※】は、付属しているメーターの種類によって異なりますので、**《メーター対応表》**を参照して、選定してください。

また、電解コンデンサは、＋ー極性がありますので、取り付ける方向に注意が必要です。長い方の足が＋で、本体にライン線が入っている方の足がーです。また、背が高い場合は、寝かせた状態に取り付けないと、シールドケースの蓋が閉らなくなるので、御注意ください。

注意がお分かりになりましたら、作業性を考慮して、背の低い部品から取り付けましょう。

レンジ選択については、基板の【Ｌ】を【ＧＮＤ】に接続すればＨＩレンジ（低感度）に、接続せずそのままにすればＬＯレンジ（高感度）に設定できます。接続箇所はすぐ隣ですので、基板裏面でハンダを多めに盛れば、簡単に接続できます。

■工作３／３■全体の組立----------

アンテナコネクタ付のシールドケース基本材に、ケース壁のみを取り付けます。この際、ケース壁の孔が、上側に並ぶようにします。これは、ケース外部に配置するメーターへの配線をし易くする為です。

まず、基板にハンダ付けされた抵抗【５１Ω】のアンテナ側の足を、成るべく短距離でアンテナ端子にハンダ付けします。

電気的に接続されていれば、そんなに丈夫にしなくとも大丈夫です。アンテナ端子は、結構折れ易いので御注意ください。

次に、【５１Ω】のアース側の足を、ケース内側にハンダ付けします。ケースは大きくて熱が逃げ易いので、なるべく熱容量の大きなハンダゴテで、素早くやるのがコツです。

ここで、ケース蓋を取り付ける前に、各種配線を基板にハンダ付けしておきます。

メーターへの配線ついては、基板の【M】とメーターの【+】を、基板の【ＧＮＤ】とメーターの【−】を、それぞれ接続します。このさい、メーターはケース外部に配置するので、配線は、ケース壁の孔を通して行います。

電源への配線については、基板の【Vcc】と００６Ｐスナップの【赤】を、基板の【ＧＮＤ】と００６Ｐスナップの【黒】を、それぞれ接続します。

ここまで出来たら、まず目視で、全体の配線チェックを行い、電池を００６Ｐスナップに接続して、ＩＣソケットへの５Ｖ電源供給をテスターなどで確認します。そして、電源を切ってから、ＩＣをソケットへ差し込みます。ＩＣには方向性があり、静電気にも弱いので御注意ください。

次に、漸く、ケース蓋を取り付けます。ところで、蓋は金属製ですから、基板下面と接触して、ショートしない様に御注意ください。なるべく間に絶縁材を配置することをお勧めします。

最後に００６Ｐ９Ｖ電池を接続して完成です。

■使用方法■

ロッドアンテナ側はＢＮＣコネクタ、ケース側はＦコネクタですので、付属の変換コネクタを介して接続します。ＢＮＣコネクタは、「カチッ」と止まるまでねじ込んで下さい。Ｆコネクタは、中心のピンを曲げない様に注意して、止まる所までねじ込んで下さい。

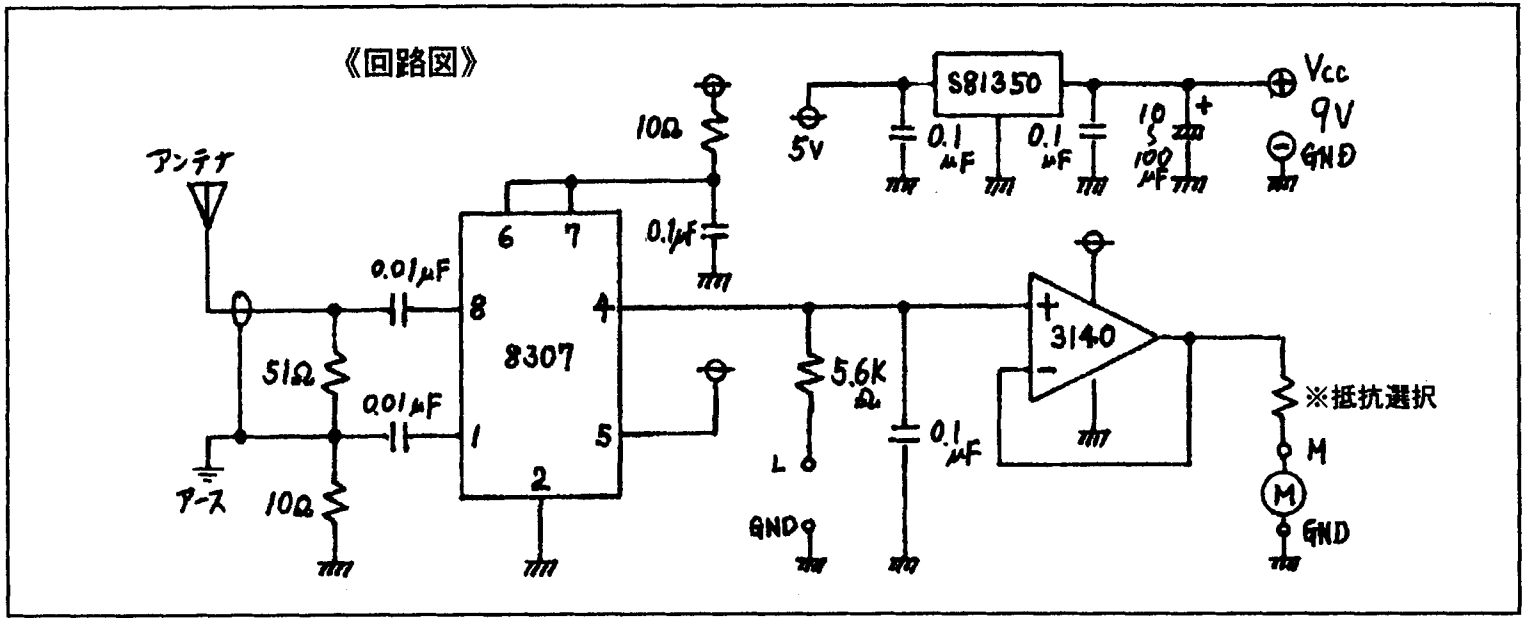
本キットは、回路も単純で、部品点数も少なく、精度が要求される部品も特にありません。従って、説明書どおりそのままストレートに組み立てれば、ほぼ同一性能の、安定した特性を得ることができます。（特に、アンテナ部とアース部の改造変更は、周波数特性に大きく影響します。）

この為、個別に調整する必要は、特になく、予め、こちらで校正して作成した、メータ目盛り（《メーター対応表》参照）を、もともと付いている、メーター目盛り盤の上に、貼って頂くだけでＯＫです（薄めの両面テープなどが便利）。

勿論、校正する為の器材をお持ちのプロの方は、個別に校正されるのも結構です。また、部品のみを使用して、オリジナル品を製作なさるのもご勝手です。

但し、本説明書に沿った組立以外の製作に関する御質問には、一切お答えできませんので、ご了承願います。

《回路図》



Low Cost DC-500 MHz, 92 dB Logarithmic Amplifier

AD8307

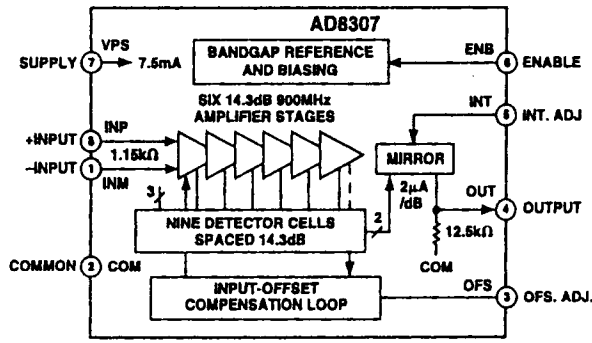
FEATURES

Complete Multistage Logarithmic Amplifier
92 dB Dynamic Range: -75 dBm to +17 dBm
To -90 dBm Using Matching Network
Single Supply of 2.7 V Min at 7.5 mA Typical
DC-500 MHz Operation, ±1 dB Linearity
Slope of 25 mV/dB, Intercept of -84 dBm
Highly Stable Scaling Over Temperature
Fully Differential DC-Coupled Signal Path
100 ns Power-Up Time, 150 µA Sleep Current

APPLICATIONS

Conversion of Signal Level to Decibel Form
Transmitter Antenna Power Measurement
Receiver Signal Strength Indication (RSSI)
Low Cost Radar and Sonar Signal Processing
Network and Spectrum Analyzers (to 120 dB)
Signal Level Determination Down to 20 Hz
True Decibel AC Mode for Multimeters

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD8307 is the first logarithmic amplifier in an 8-lead (SO-8) package. It is a complete 500 MHz monolithic demodulating logarithmic amplifier based on the progressive compression (successive detection) technique, providing a dynamic range of 92 dB to ±3 dB law-conformance and 88 dB to a tight ±1 dB error bound at all frequencies up to 100 MHz. It is extremely stable and easy to use, requiring no significant external components. A single supply voltage of 2.7 V to 5.5 V at 7.5 mA is needed, corresponding to an unprecedented power consumption of only 22.5 mW at 3 V. A fast-acting CMOS-compatible control pin can disable the AD8307 to a standby current of under 150 µA.

Each of the cascaded amplifier/limiter cells has a small-signal gain of 14.3 dB, with a -3 dB bandwidth of 900 MHz. The input is fully differential and at a moderately high impedance (1.1 kΩ in parallel with about 1.4 pF). The AD8307 provides a basic dynamic range extending from approximately -75 dBm (where dBm refers to a 50 Ω source, that is, a sine amplitude of -85 dBV or about ±56 µV) up to +17 dBm (a sine amplitude of +6.8 dBV or ±2.2 V). A simple input-matching network can lower this range to -88 dBm to +3 dBm. The logarithmic linearity is typically within ±0.3 dB up to 100 MHz over the central portion of this range, and is degraded only slightly at 500 MHz. There is no minimum frequency limit; the AD8307 may be used at audio frequencies (20 Hz) or even lower.

The output is a voltage scaled 25 mV/dB, generated by a current of nominally 2 µA/dB through an internal 12.5 kΩ resistor. This voltage varies from 0.25 V at an input of -74 dBm (that is, the ac intercept is at -84 dBm, a 20 µV rms sine input), up to 2.5 V for an input of +16 dBm. This slope and intercept can be trimmed using external adjustments. Using a 2.7 V supply, the output scaling may be lowered, for example to 15 mV/dB, to permit utilization of the full dynamic range.

The AD8307 exhibits excellent supply insensitivity and temperature stability of the scaling parameters. The unique combination of low cost, small size, low power consumption, high accuracy and stability, very high dynamic range, and a frequency range encompassing audio through IF to UHF, make this product useful in numerous applications requiring the reduction of a signal to its decibel equivalent.

The AD8307 is available in the industrial temperature range of -40°C to +85°C, and in 8-lead SOIC and PDIP packages.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... +7.5 V
Input Voltage (Pins 1, 8) ..... V_{SUPPLY}
Storage Temperature Range, N, R ..... -65°C to +125°C
Ambient Temperature Range, Rated Performance Industrial,
AD8307AN, AD8307AR ..... -40°C to +85°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

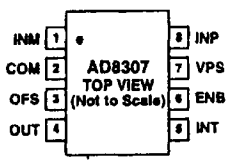
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD8307AR	-40°C to +85°C	SOIC	R-8
AD8307AN	-40°C to +85°C	Plastic DIP	N-8

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8307 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Name	Function
1	INM	Signal Input, Minus Polarity; Normally at $V_{POS}/2$.
2	COM	Common Pin (Usually Grounded).
3	OFS	Offset Adjustment; External Capacitor Connection.
4	OUT	Logarithmic (RSSI) Output Voltage; R_{OUT} = 12.5 kΩ.
5	INT	Intercept Adjustment; ±6 dB (See Text).
6	ENB	CMOS-compatible Chip Enable; Active when "HI."
7	VPS	Positive Supply, 2.7 V-5.5 V.
8	INP	Signal Input, Plus Polarity; Normally at $V_{POS}/2$. Note: Due to the symmetrical nature of the response, there is no special significance to the sign of the two input pins. DC resistance from INP to INM = 1.1 kΩ.

AD8307–SPECIFICATIONS (V_S = +5 V, T_A = 25°C, $R_L \geq 1$ MΩ, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
GENERAL CHARACTERISTICS					
Input Range (±1 dB Error)	Expressed in dBm re 50 Ω	-72		16	dBm
Logarithmic Conformance	f ≤ 100 MHz, Central 80 dB		±0.3	±1	dB
	f = 500 MHz, Central 75 dB		±0.5		dB
Logarithmic Slope	Unadjusted[1]	23	25	27	mV/dB
vs. Temperature		23		27	mV/dB
Logarithmic Intercept	Sine Amplitude; Unadjusted[2]		20		μV
	Equivalent Sine Power in 50 Ω	-87	-84	-77	dBm
vs. Temperature		-88		-76	dBm
Input Noise Spectral Density	Inputs Shorted		1.5		$nV/\sqrt{Hz}$
Operating Noise Floor	R_{SOURCE} = 50 Ω/2		-78		dBm
Output Resistance	Pin 4 to Ground	10	12.5	15	kΩ
Internal Load Capacitance			3.5		pF
Response Time	Small Signal, 10%-90%, 0 mV–100 mV, C_L = 2 pF		400		ns
	Large Signal, 10%-90%, 0 V–2.4 V, C_L = 2 pF		500		ns
Upper Usable Frequency[3]			500		MHz
Lower Usable Frequency	Input AC-Coupled		10		Hz
AMPLIFIER CELL CHARACTERISTICS					
Cell Bandwidth	-3 dB		900		MHz
Cell Gain			14.3		dB
INPUT CHARACTERISTICS					
DC Common-Mode Voltage	Inputs AC-Coupled		3.2		V
Common-Mode Range	Either Input (Small Signal)	-0.3	1.6	V_S - 1	V
DC Input Offset Voltage[4]	$R_{SOURCE} \leq 50$ Ω		50	500	μV
	Drift		0.8		μV/°C
Incremental Input Resistance	Differential		1.1		kΩ
Input Capacitance	Either Pin to Ground		1.4		pF
Bias Current	Either Input		10	25	μA
POWER INTERFACES					
Supply Voltage		2.7		5.5	V
Supply Current	$V_{ENB} \geq 2$ V		8	10	mA
Disabled	$V_{ENB} \leq 1$ V		150	750	μA

NOTES

[1]This may be adjusted downward by adding a shunt resistor from the Output to Ground. A 50 kΩ resistor will reduce the nominal slope to 20 mV/dB.

[2]This may be adjusted in either direction by a voltage applied to Pin 5, with a scale factor of 8 dB/V.

[3]See Application on 900 MHz operation.

[4]Normally nulled automatically by internal offset correction loop. May be manually nulled by a voltage applied between Pin 3 and Ground; see APPLICATIONS.

Specifications subject to change without notice.

AD8307–Typical Performance Characteristics

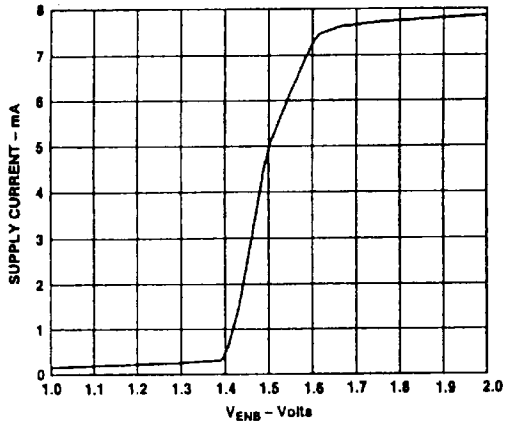


Figure 1. Supply Current vs. V_{ENB} Voltage (5 V)

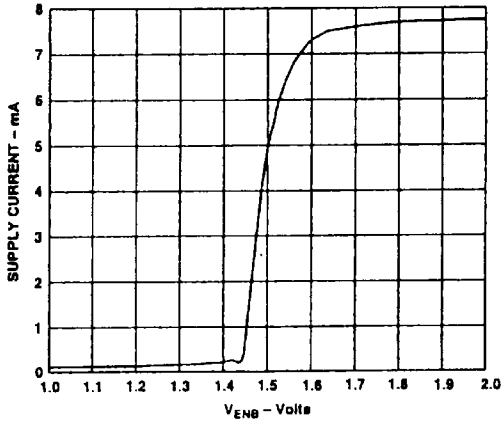


Figure 2. Supply Current vs. V_{ENB} Voltage (3 V)

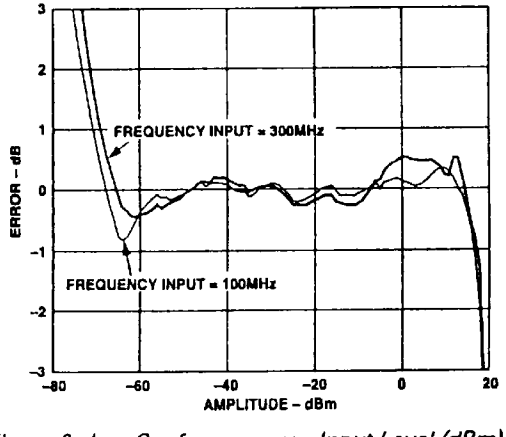


Figure 3. Log Conformance vs. Input Level (dBm) @ 100 MHz, 300 MHz

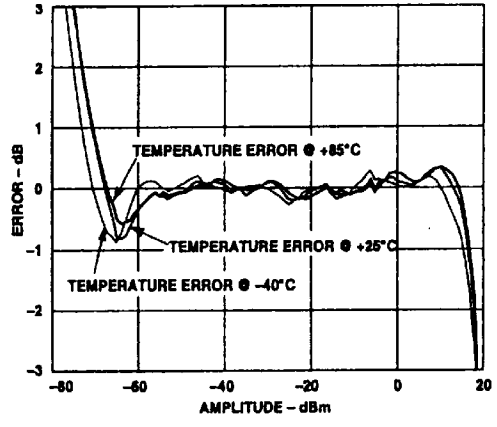


Figure 4. Log Conformance vs. Input Level (dBm) at 25°C, 85°C, -40°C

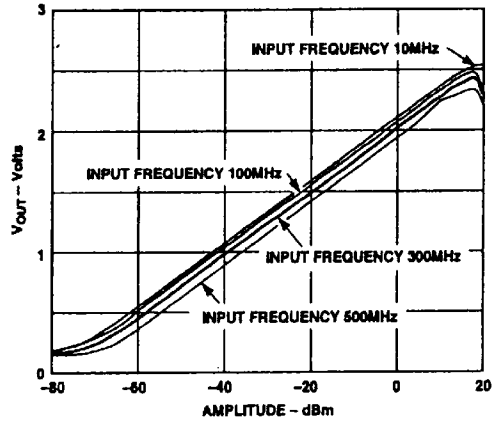


Figure 5. V_{OUT} vs. Input Level (dBm) at Various Frequencies

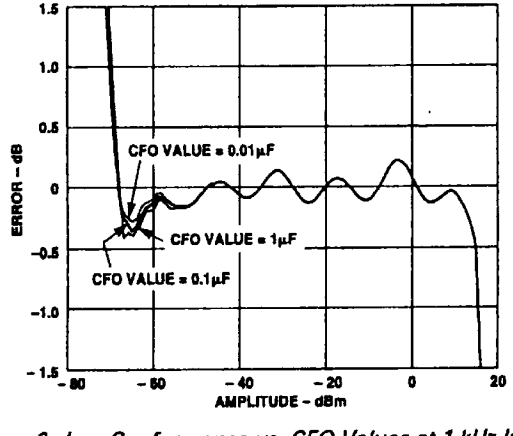


Figure 6. Log Conformance vs. CFO Values at 1 kHz Input Frequency

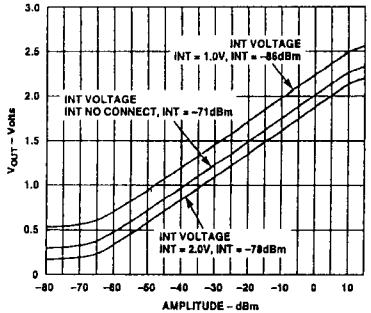


Figure 8. V_{OUT} vs. Input Level at 3 V Supply Using AD820 as Buffer, Gain = +2; Showing Intercept Adjustment

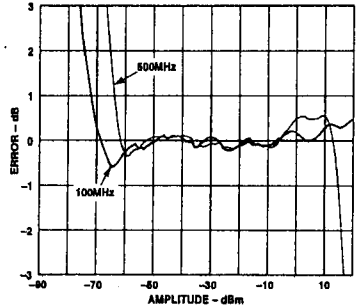


Figure 11. Log Conformance vs. Input at 100 MHz, 500 MHz; Input Driven Differentially Using Transformer

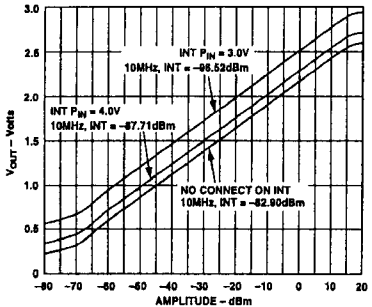


Figure 7. V_{OUT} vs. Input Level at 5 V Supply; Showing Intercept Adjustment

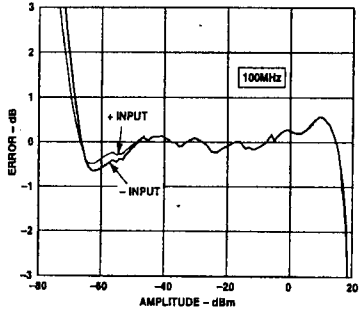


Figure 10. Log Conformance vs. Input Level at 100 MHz; Showing Response to Alternative Inputs

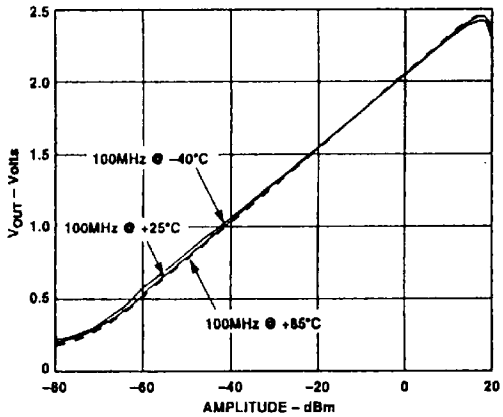


Figure 9. V_{OUT} vs. Input Level at Three Temperatures (–40°C, +25°C, +85°C)

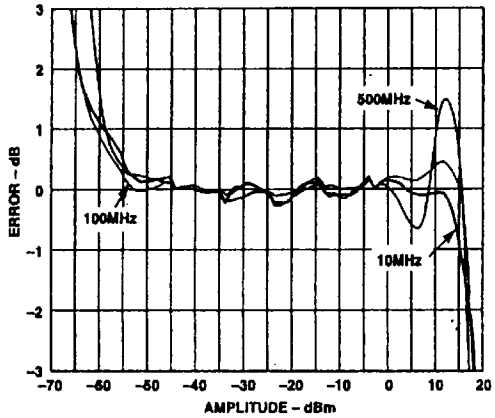


Figure 12. Log Conformance vs. Input Level at 3 V Supply Using AD820 as Buffer, Gain = +2

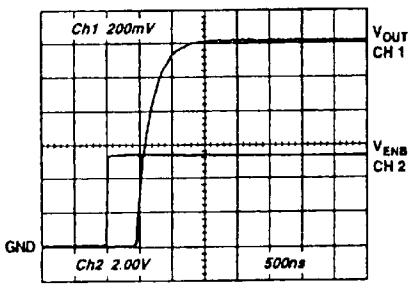


Figure 13. Power-Up Response Time

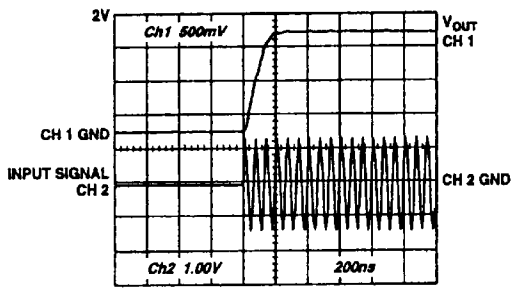


Figure 16. V_{OUT} Rise Time

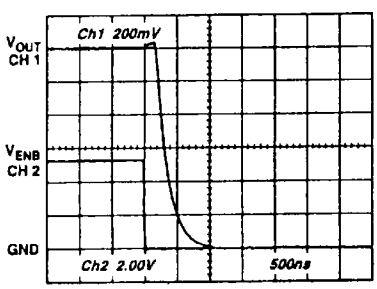


Figure 14. Power-Down Response Time

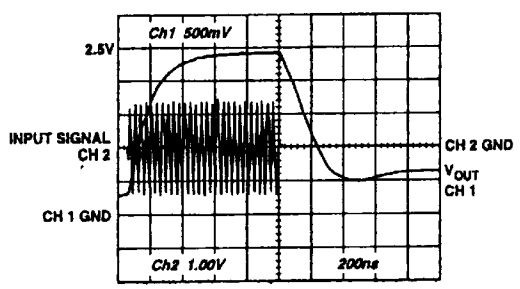


Figure 17. Large Signal Response Time

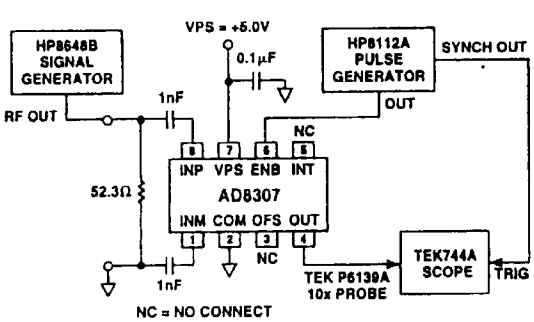


Figure 15. Test Setup For Power-Up/Power-Down Response Time

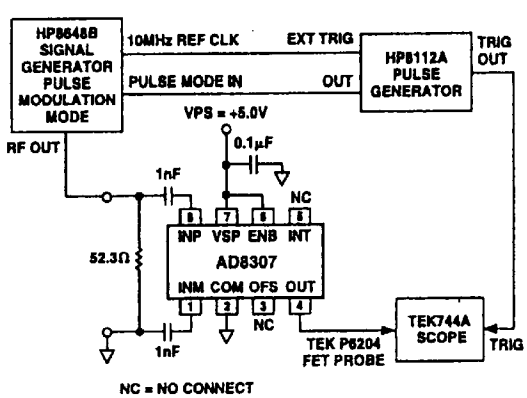


Figure 18. Test Setup For V_{OUT} Pulse Response

PRODUCT OVERVIEW

The AD8307 comprises six main amplifier/limiter stages, each having a gain of 14.3 dB and small signal bandwidth of 900 MHz; the overall gain is 86 dB with a -3 dB bandwidth of 500 MHz. These six cells, and their associated g_m-styled full-wave detectors, handle the lower two-thirds of the dynamic range. Three top-end detectors, placed at 14.3 dB taps on a passive attenuator, handle the upper third of the 90 dB range. Biasing for these cells is provided by two references: one determines their gain; the other is a bandgap circuit that determines the logarithmic slope and stabilizes it against supply- and temperature-variations. The AD8307 may be enabled/disabled by a CMOS-compatible level at ENB (Pin 6). The first amplifier stage provides a low voltage noise spectral density (1.5 nV/$\sqrt{\text{Hz}}$).

The differential current-mode outputs of the nine detectors are summed and then converted to single-sided form in the output stage, nominally scaled 2 μA/dB. The logarithmic output voltage is developed by applying this current to an on-chip 12.5 kΩ resistor, resulting in a logarithmic slope of 25 mV/dB (i.e., 500 mV/decade) at OUT. This voltage is not buffered, allowing the use of a variety of special output interfaces, including the addition of post-demodulation filtering. The last detector stage includes a modification to temperature-stabilize the log intercept, which is accurately positioned to make optimal use of the full output voltage range available. The intercept may be adjusted using the pin INT, which adds or subtracts a small current to the signal current.

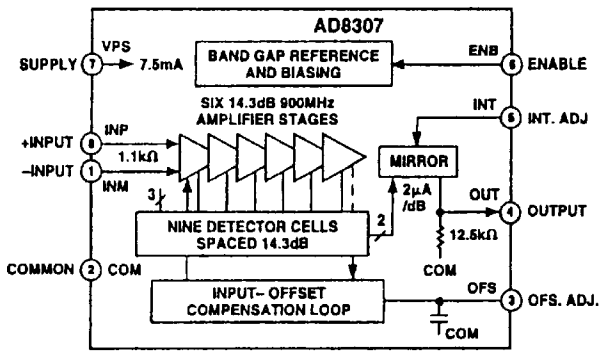


Figure 25. Main Features of the AD8307

The last gain stage also includes an offset-sensing cell. This generates a bipolarity output current when the main signal path has an imbalance due to accumulated dc offsets. This current is integrated by an on-chip capacitor (which may be increased in value by an off-chip component, at OFS). The resulting voltage is used to null the offset at the output of the first stage. Since it does not involve the signal input connections, whose ac coupling capacitors otherwise introduce a second pole in the feedback path, the stability of the offset correction loop is assured.

The AD8307 is built on an advanced dielectrically-isolated complementary bipolar process. Most resistors are thin-film types having a low temperature coefficient of resistance (TCR) and high linearity under large signal conditions. Their absolute tolerance will typically be within ±20%. Similarly, the capacitors have a typical tolerance of ±15% and essentially zero temperature or voltage sensitivity. Most interfaces have additional small junction capacitances associated with them, due to active devices or ESD protection; these may be neither accurate nor stable. Component numbering in each of these interface diagrams is local.

Enable Interface

The chip-enable interface is shown in Figure 26. The currents in the diode-connected transistors control the turn-on and turn-off states of the bandgap reference and the bias generator, and are a maximum of 100 μA when Pin 6 is taken to 5 V, under worst case conditions. Left unconnected, or at a voltage below 1 V, the AD8307 will be disabled and consume a sleep current of under 50 μA; tied to the supply, or a voltage above 2 V, it will be fully enabled. The internal bias circuitry is very fast (typically <100 ns for either OFF or ON), and in practice the latency period before the log amp exhibits its full dynamic range is more likely to be limited by factors relating to the use of ac coupling at the input or the settling of the offset-control loop (see following sections).

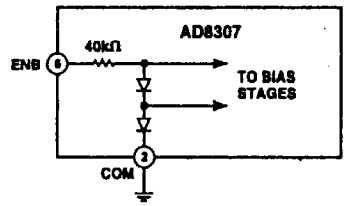


Figure 26. Enable Interface

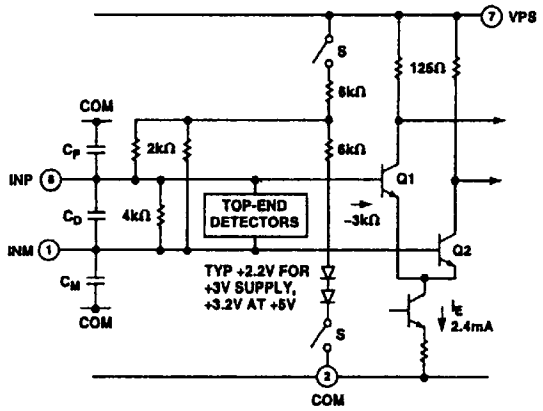


Figure 27. Signal Input Interface

Input Interface

Figure 27 shows the essentials of the signal input interface. C_P and C_M are the parasitic capacitances to ground; C_D is the differential input capacitance, mostly due to Q1 and Q2. In most applications both input pins are ac-coupled. The switches S close when Enable is asserted. When disabled, the inputs float, bias current I_E is shut off, and the coupling capacitors remain charged. If the log amp is disabled for long periods, small leakage currents will discharge these capacitors. If they are poorly matched, charging currents at power-up can generate a transient input voltage which may block the lower reaches of the dynamic range until it has become much less than the signal.

In most applications, the signal will be single-sided, and may be applied to either Pin 1 or Pin 8, with the other pin ac-coupled to ground. Under these conditions, the largest input signal that can be handled by the AD8307 is +10 dBm (sine amplitude of ±1 V) when operating from a 3 V supply; a +16 dBm may be handled using a 5 V supply. The full 16 dBm may be achieved for supplies down to 2.7 V, using a fully balanced drive. For frequencies above about 10 MHz, this is most easily achieved using a matching network (see below). Using such a network, having an inductor at the input, the input transient noted above is eliminated. Occasionally, it may be desirable to use the dc-coupled potential of the AD8307. The main challenge here is to present signals to the log amp at the elevated common-mode input level, requiring the use of low noise, low offset buffer amplifiers. Using dual supplies of ±3 V, the input pins may operate at ground potential.

Offset Interface

The input-referred dc offsets in the signal path are nulled via the nterface associated with Pin 3, shown in Figure 28. Q1 and Q2 ire the first stage input transistors, with their corresponding oad resistors (125 Ω). Q3 and Q4 generate small currents, which can introduce a dc offset into the signal path. When the /oltage on OFS is at about 1.5 V, these currents are equal, and ıominally 16 μA. When OFS is taken to ground, Q4 is off and :he effect of the current in Q3 is to generate an offset voltage of 16 μA × 125 Ω = 2 mV. Since the first stage gain is ×5, this is :quivalent to a input offset (INP to INM) of 400 μV. When DFS is taken to its most positive value, the input-referred offset s reversed, to −400 μV. If true dc-coupling is needed, down to /ery small inputs, this automatic loop must be disabled, and the esidual offset eliminated using a manual adjustment, as explained n the next section.

n normal operation, however, using an ac-coupled input signal, he OFS pin should be left open. Any residual input-offset volt- ıge is then automatically nulled by the action of the feedback oop. The g_m cell, which is gated off when the chip is disabled, :onverts any output offset (sensed at a point near the end of the :ascade of amplifiers) to a current. This is integrated by the on- :hip capacitor C_{HP}, plus any added external capacitance C_{OFS}, o as to generate an error voltage, which is applied back to the nput stage in the polarity needed to null the output offset. From ı small-signal perspective, this feedback alters the response of he amplifier, which, rather than behaving as a fully dc-coupled ystem, now exhibits a zero in its ac transfer function, resulting n a closed-loop high-pass corner at about 700 kHz.

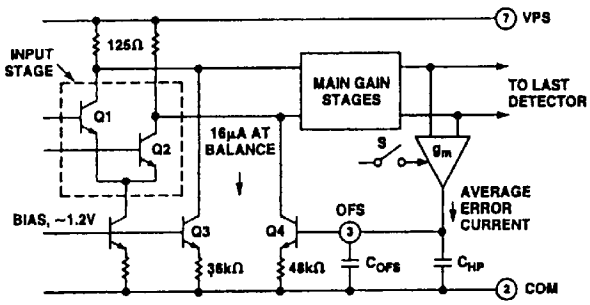


Figure 28. Offset Interface and Offset-Nulling Path

The offset feedback is limited to a range ±400 μV; signals larger than this override the offset control loop, which only impacts performance for very small inputs. An external capacitor reduces the high pass corner to arbitrarily low frequencies; using 1 μF this corner is below 10 Hz. All ADI log amps use an offset-nulling loop; the AD8307 differs in using this single-sided form.

Output Interface

The outputs from the nine detectors are differential currents, having an average value that is dependent on the signal input level, plus a fluctuation at twice the input frequency. The currents are summed at nodes LGP and LGN in Figure 29. Further currents are added at these nodes, to position the intercept, by slightly raising the output for zero input, and to provide temperature compensation. Since the AD8307 is not laser-trimmed, there is a small uncertainty in both the log slope and the log intercept. These scaling parameters may be adjusted (see below).

For zero-signal conditions, all the detector output currents are equal. For a finite input, of either polarity, their difference is converted by the output interface to a single-sided unipolar current nominally scaled 2 μA/dB (40 μA/decade), at the output pin OUT. An on-chip 12.5 kΩ resistor, R1, converts this current to a voltage of 25 mV/dB. C1 and C2 are effectively in shunt with R1 and form a low-pass filter pole, with a corner frequency of about 5 MHz. The pulse response settles to within 1% of the final value within 300 ns. This integral low-pass filter provides adequate smoothing in many IF applications. At 10.7 MHz, the 2f ripple is 12.5 mV in amplitude, equivalent to ±0.5 dB, and only 0.5 mV (±0.02 dB) at f = 50 MHz. A filter capacitor C_{FLT} added from OUT to ground will lower this corner frequency. Using 1 μF, the ripple is maintained to less than ±0.5 dB down to input frequencies of 100 Hz. Note that C_{OFS} (above) should also be increased in low frequency applications, and will typically be made equal to C_{FLT}.

It may be desirable to increase the speed of the output response, with the penalty of increased ripple. One way to do this is simply by connecting a shunt load resistor from OUT to ground, which raises the low pass corner frequency. This also alters the logarithmic slope, for example to 7.5 mV/dB using a 5.36 kΩ resistor, while reducing the 10%-90% rise time to 25 ns. The ripple amplitude for 50 MHz input remains 0.5 mV, but this is now equivalent to ±0.07 dB. If a negative supply is available, the output pin may be connected directly to the summing node of an external op amp connected as an inverting-mode transresistance stage.

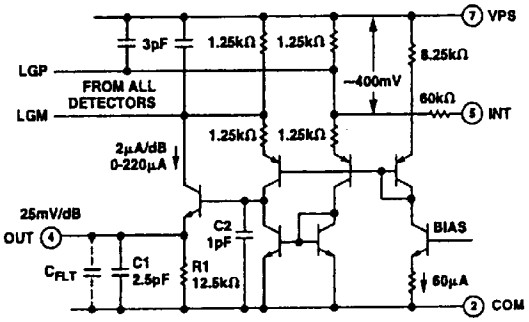


Figure 29. Simplified Output Interface

Narrow-Band Matching

Transformer coupling is useful in broadband applications. However, a magnetically-coupled transformer may not be convenient in some situations. At high frequencies, it is often preferable to use a narrow-band matching network, as shown in Figure 33. This has several advantages. The same voltage gain is achieved, providing increased sensitivity, but now a measure of selectivity is also introduced. The component count is low: two capacitors and an inexpensive chip inductor. Further, by making these capacitors unequal the amplitudes at INP and INM may be equalized when driving from a single-sided source; that is, the network also serves as a balun. Figure 34 shows the response for a center frequency of 100 MHz; note the very high attenuation at low frequencies. The high-frequency attenuation is due to the input capacitance of the log amp.

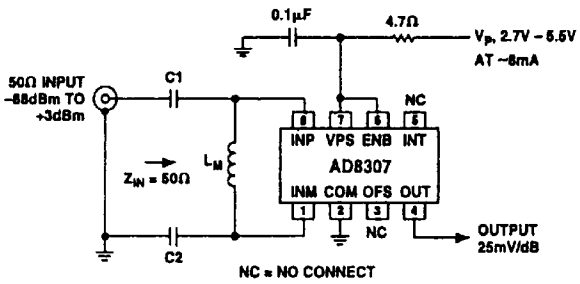


Figure 33. High Frequency Input Matching Network

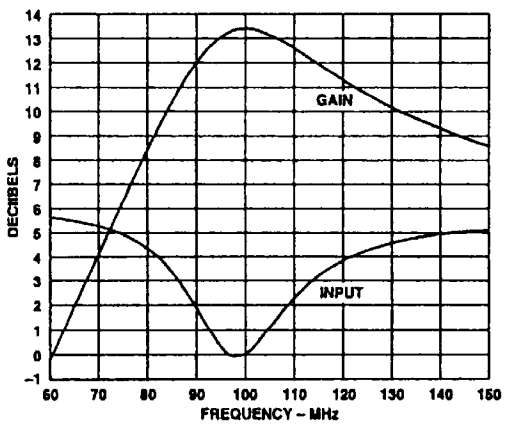


Figure 34. Response of 100 MHz Matching Network

Table I provides solutions for a variety of center frequencies F_C and matching impedances Z_{IN} of nominally 50 Ω and 100 Ω. The unequal capacitor values were chosen to provide a well-balanced differential drive, and also to allow better centering of the frequency response peak when using standard value components; this generally results in a Z_{IN} that is not exact. The full AD8307 HF input impedance and the inductor losses were included in the modeling.

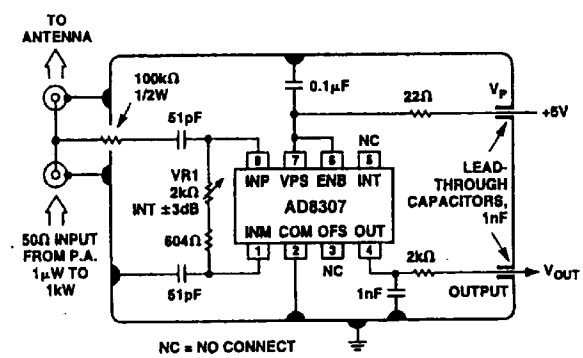


Figure 39. 1 µW to 1 kW 50-Ω Power Meter

Table I. Narrow-Band Matching Values

F_C MHz	Z_{IN} Ω	C1 pF	C2 pF	L_M nH	Voltage Gain (dB)
10	45	160	150	3300	13.3
20	44	82	75	1600	13.4
50	46	30	27	680	13.4
100	50	15	13	330	13.4
150	57	10	8.2	220	13.2
200	57	7.5	6.8	150	12.8
250	50	6.2	5.6	100	12.3
500	54	3.9	3.3	39	10.9
10	103	100	91	5600	10.4
20	102	51	43	2700	10.4
50	99	22	18	1000	10.6
100	98	11	9.1	430	10.5
150	101	7.5	6.2	260	10.3
200	95	5.6	4.7	180	10.3
250	92	4.3	3.9	130	9.9
500	114	2.2	2.0	47	6.8

Slope and Intercept Adjustments

Where higher calibration accuracy is needed, the adjustments shown in Figure 35 can be used, either singly or in combination. The log slope is lowered to 20 mV/dB by shunting the nominally 12.5 kΩ on-chip load resistor (see Figure 29) with 50 kΩ, adjusted by VR1. The calibration range is ±10% (18 mV/dB to 22 mV/dB), including full allowance for the variability in the value of the internal load. The adjustment may be made by alternately applying two input levels, provided by an accurate signal generator, spaced over the central portion of the log amp's dynamic range, for example –60 dBm and 0 dBm. An AM-modulated signal, at the center of the dynamic range, can also be used. For a modulation depth M, expressed as a fraction, the decibel range between the peaks and troughs over one cycle of the modulation period is given by:

$$\Delta\ dB = 20 \log_{10} \frac{1+M}{1-M} \qquad (7)$$

For example, using an rms signal level of –40 dBm with a 70% modulation depth (M = 0.7), the decibel range is 15 dB, as the signal varies from –47.5 dBm to –32.5 dBm.

The log intercept is adjustable over a ±3 dB range, which is sufficient to absorb the worst-case intercept error in the AD8307 plus some system-level errors. For greater range, set R_S to zero. VR2 is adjusted while applying an accurately known CW signal near the lower end of the dynamic range, in order to minimize the effect of any residual uncertainty in the slope. For example, to position the intercept to –80 dBm, a test level of –65 dBm may be applied and VR2 adjusted to produce a dc output of 15 dB above zero at 25 mV/dB, which is +0.3 V.

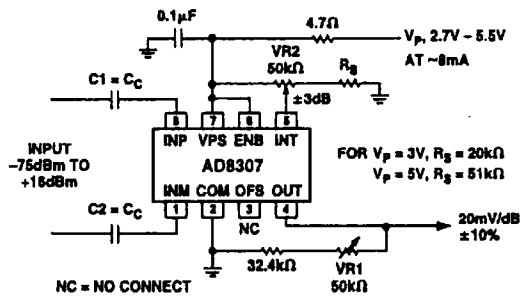


Figure 35. Slope and Intercept Adjustments